

# FDMS6681Z

## MOSFET – POWERTRENCH<sup>®</sup>, P-Channel

**-30 V, -122 A, 3.2 mΩ**

### General Description

The FDMS6681Z has been designed to minimize losses in load switch applications. Advancements in both silicon and package technologies have been combined to offer the lowest  $r_{DS(on)}$  and ESD protection.

### Features

- Max  $r_{DS(on)}$  = 3.2 mΩ at  $V_{GS} = -10$  V,  $I_D = -21.1$  A
- Max  $r_{DS(on)}$  = 5.0 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -15.7$  A
- Advanced Package and Silicon Combination for Low  $r_{DS(on)}$
- HBM ESD Protection Level of 8 kV Typical (Note 3)
- MSL1 Robust Package Design
- RoHS Compliant

### Applications

- Load Switch in Notebook and Server
- Notebook Battery Pack Power Management

### MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain to Source Voltage	-30	V
$V_{GS}$	Gate to Source Voltage	±25	V
$I_D$	Drain Current – Continuous $T_C = 25^\circ\text{C}$ (Note 5)	-122	A
	– Continuous $T_C = 100^\circ\text{C}$ (Note 5)	-77	
	– Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	-21.1	
	– Pulsed (Note 4)	-600	
$P_D$	Power dissipation $T_C = 25^\circ\text{C}$	73	W
	Power dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.5	
$T_J$ , $T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

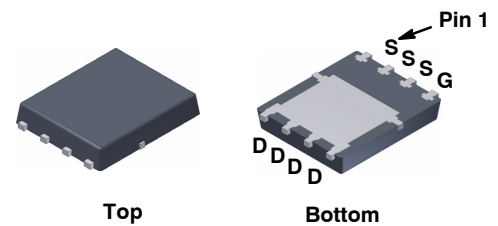
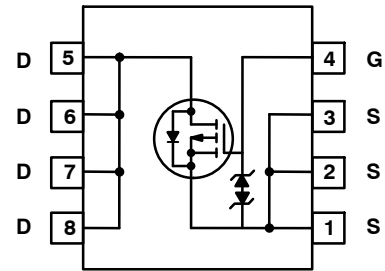
### THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.7	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	



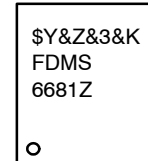
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Power 56 (PQFN8)  
CASE 483AE

### MARKING DIAGRAM



\$Y = ON Semiconductor Logo  
 &Z = Assembly Plant Code  
 &3 = Numeric Date Code  
 &K = Lot Code  
 FDMS6681Z = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FDMS6681Z

## PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Shipping <sup>†</sup>
FDMS6681Z	FDMS6681Z	Power 56	3000 Units/Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = -250 μA, V <sub>GS</sub> = 0 V	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = -250 μA, referenced to 25°C		20		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -24 V, V <sub>GS</sub> = 0 V			-1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±25 V, V <sub>DS</sub> = 0 V			±10	μA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250 μA	-1	-1.7	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = -250 μA, referenced to 25°C		-7		mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -22.1 A		2.7	3.2	mΩ
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -15.7 A		4.0	5.0	
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -22.1 A, T <sub>J</sub> = 125°C		3.9	5.0	
g <sub>FS</sub>	Forward Transconductance	V <sub>DD</sub> = -10 V, I <sub>D</sub> = -22.1 A		143		S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 0 V, f = 1MHz		7803	10380	pF
C <sub>oss</sub>	Output Capacitance			1540	2050	
C <sub>rss</sub>	Reverse Transfer Capacitance			1345	2020	

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn – On Delay Time	V <sub>DD</sub> = -15 V, I <sub>D</sub> = -22.1 A, V <sub>GS</sub> = -10 V, R <sub>GEN</sub> = 6 Ω		15	24	ns
t <sub>r</sub>	Rise Time			38	61	
t <sub>d(off)</sub>	Turn – Off Delay Time			260	416	
t <sub>f</sub>	Fall Time			197	316	
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to -10 V	V <sub>DD</sub> = -15 V, I <sub>D</sub> = -22.1 A	172	241	nC
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to -5 V		97	136	
Q <sub>gs</sub>	Gate to Source Charge			22		
Q <sub>gd</sub>	Gate to Drain “Miller” Charge			46		

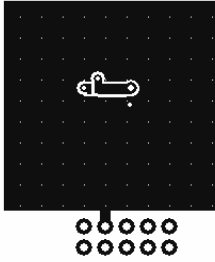
### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -2.1 A (Note 2)		0.68	1.2	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = -22.1 A (Note 2)		0.79	1.25	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = -22.1 A, di/dt = 100 A/μs		44	71	ns
Q <sub>rr</sub>	Reverse Recovery Charge			39	63	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 50°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
4. Pulsed  $I_D$  please refer to Figure 12 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal electro-mechanical application board design.

TYPICAL CHARACTERISTICS  $T_J = 25^\circ\text{C}$  unless otherwise noted

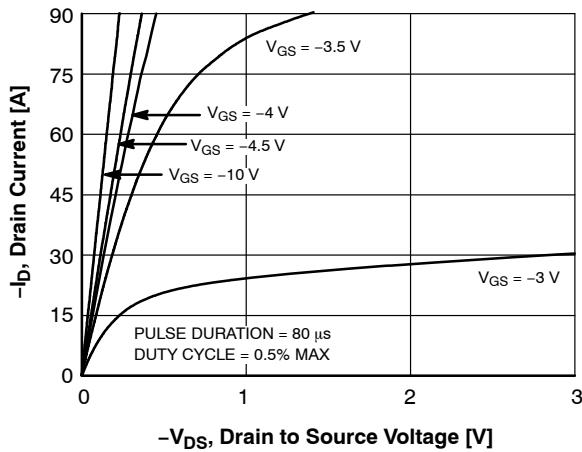


Figure 1. On Region Characteristics

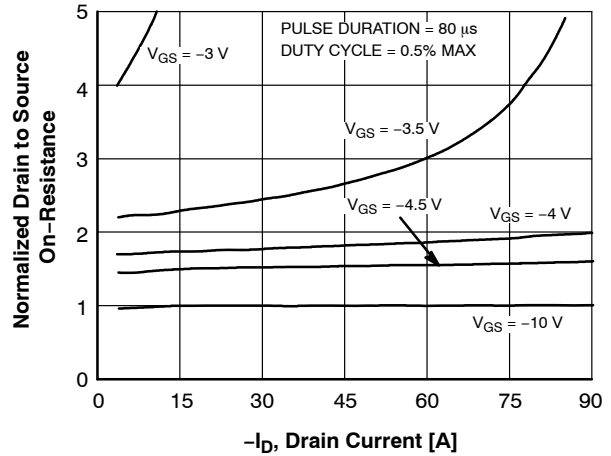


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

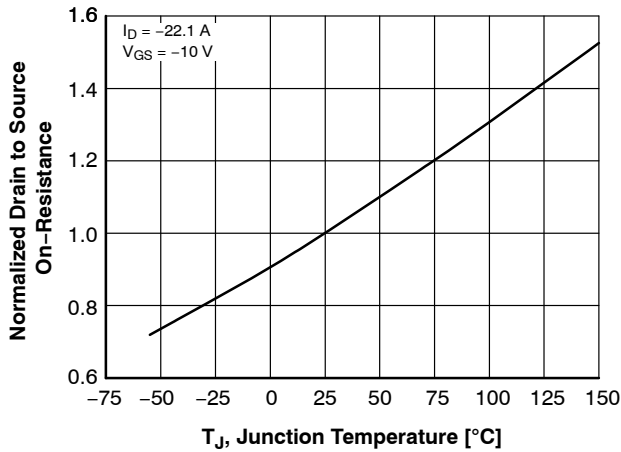


Figure 3. Normalized On Resistance vs. Junction Temperature

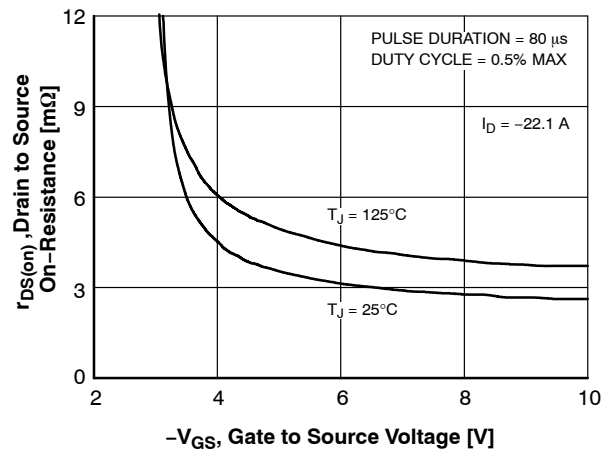


Figure 4. On-Resistance vs. Gate to Source Voltage

TYPICAL CHARACTERISTICS  $T_J = 25^\circ\text{C}$  unless otherwise noted (continued)

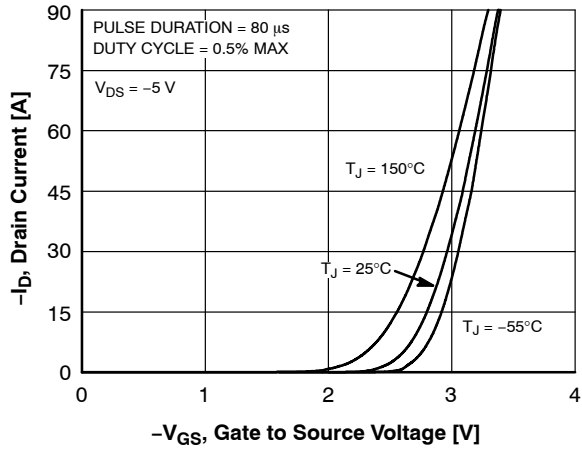


Figure 5. Transfer Characteristics

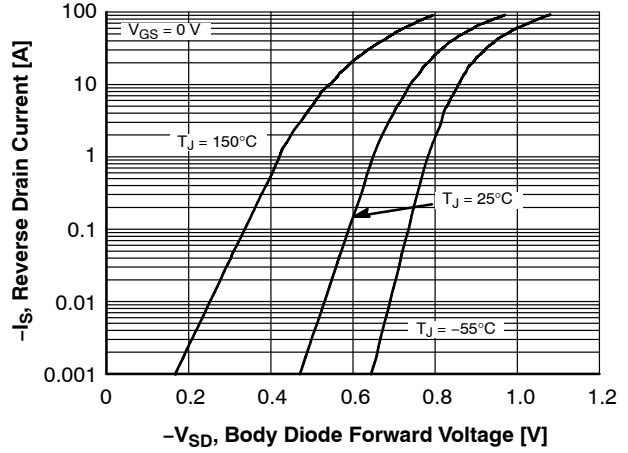


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

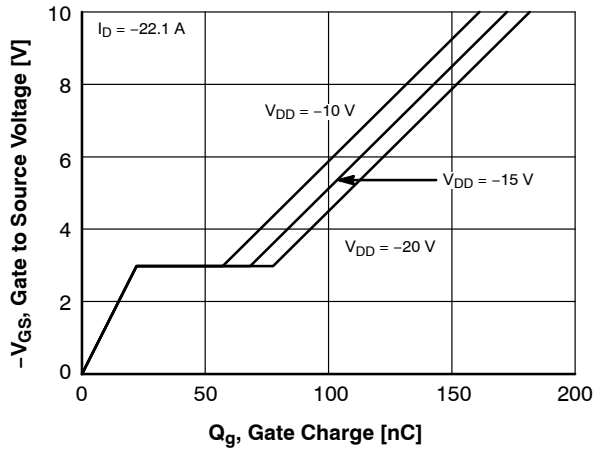


Figure 7. Gate Charge Characteristics

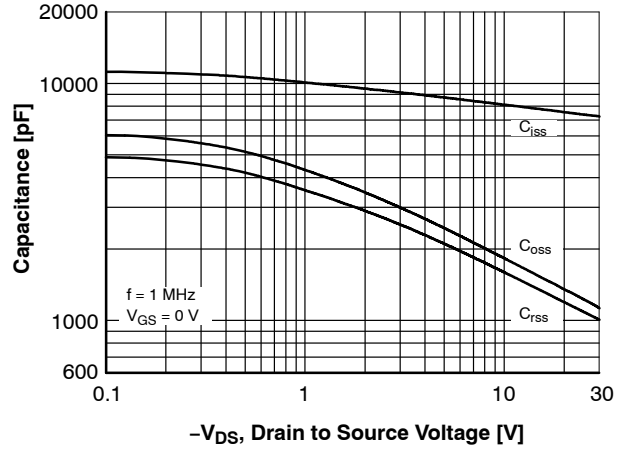


Figure 8. Capacitance vs. Drain to Source Voltage

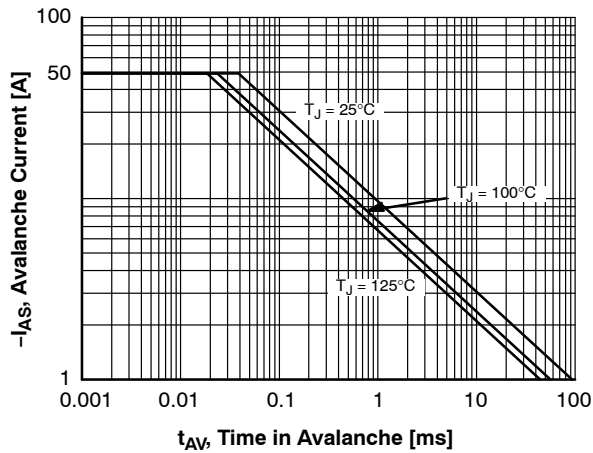


Figure 9. Unclamped Inductive Switching Capability

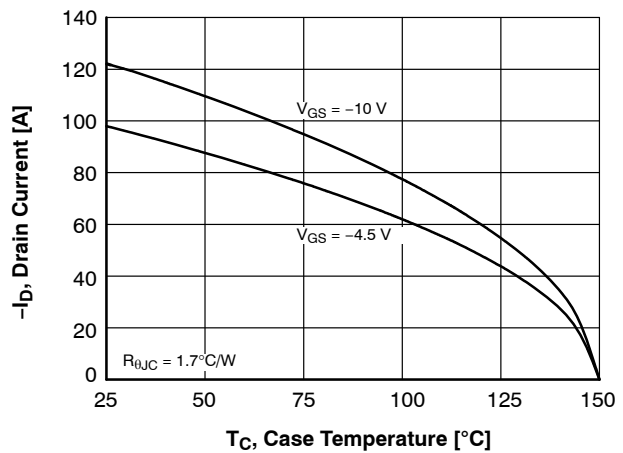


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

TYPICAL CHARACTERISTICS  $T_J = 25^\circ\text{C}$  unless otherwise noted (continued)

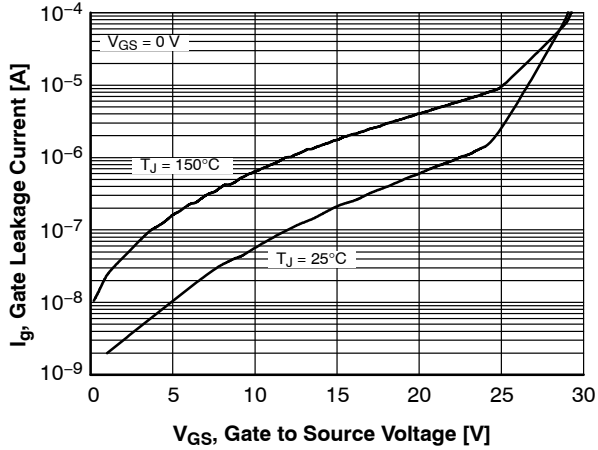


Figure 11.  $I_{gss}$  vs.  $V_{gss}$

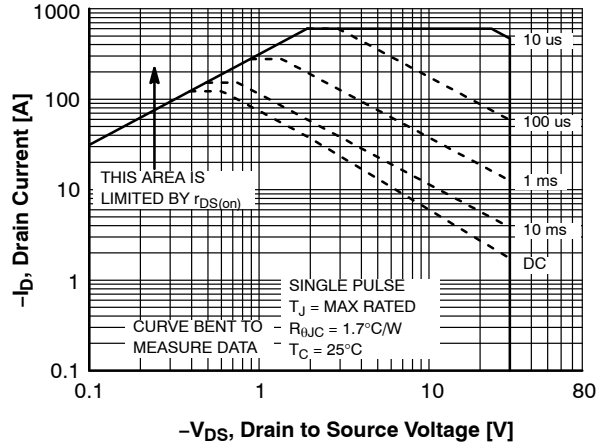


Figure 12. Forward Bias Safe Operating Area

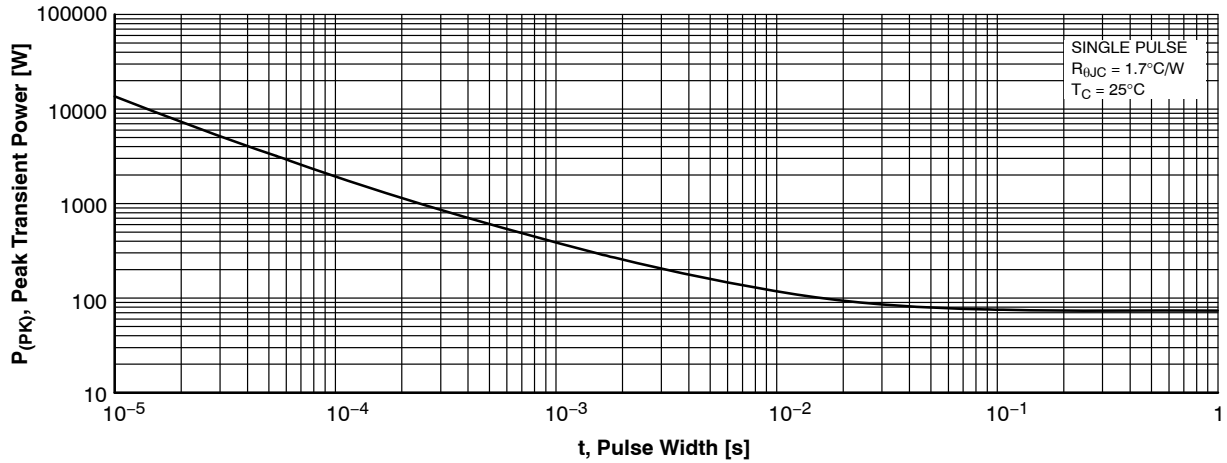


Figure 13. Single Pulse Maximum Power Dissipation

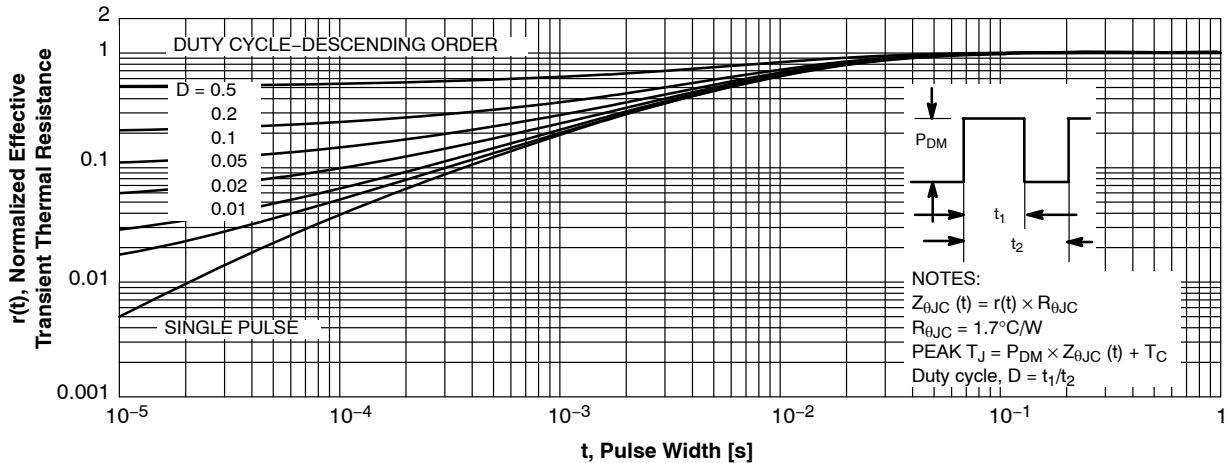
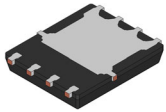


Figure 14. Transient Thermal Response Curve

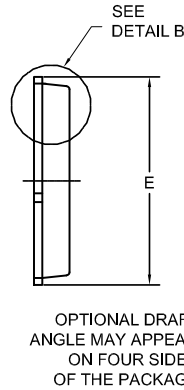
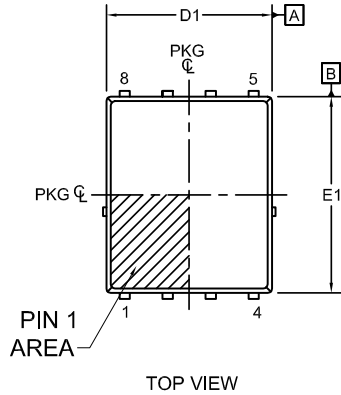
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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



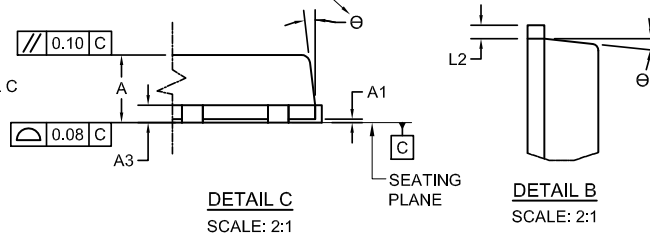
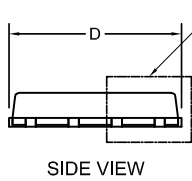
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CASE 483AE  
ISSUE C

DATE 21 JAN 2022

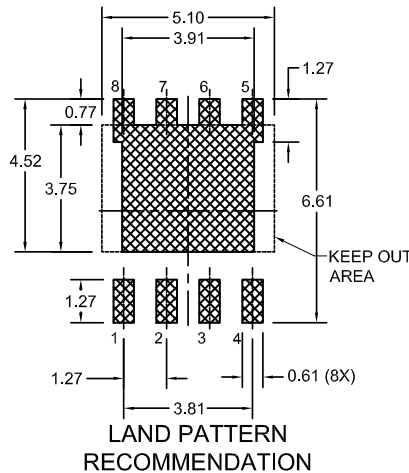
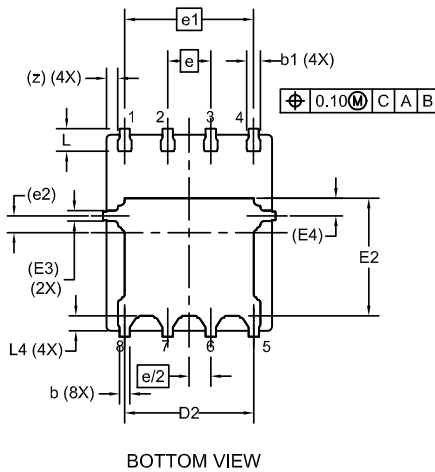


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
θ	0°	-	12°



\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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