

采用 0402 封装的低钳位电压 ESD351 单通道 30kV ESD 保护二极管

1 特性

- IEC 61000-4-2 4 级静电放电 (ESD) 保护
 - $\pm 30\text{kV}$ 接触放电
 - $\pm 30\text{kV}$ 气隙放电
- IEC 61000-4-4 瞬态放电 (EFT) 保护
 - 80A (5/50ns)
- IEC 61000-4-5 浪涌保护
 - 6A (8 μs /20 μs)
- IO 电容: 1.8pF (典型值)
- 直流击穿电压: 4.5V (最小值)
- 低泄漏电流 0.1nA (典型值)
- 极低 ESD 钳位电压
 - 在 16A TLP 下为 6.5V (I/O 引脚至 GND)
 - R_{DYN} : 0.1 Ω (I/O 引脚至 GND)
- 工业温度范围: -40°C 至 $+125^{\circ}\text{C}$
- 行业标准的 0402 封装 (DFN1006P2)

2 应用

- 终端设备
 - 可穿戴产品
 - 工业和服务机器人
 - 便携式计算机和台式机
 - 手机和平板电脑
 - 机顶盒
 - 数字视频录像机 (DVR) 和网络视频录像机 (NVR)
 - 电视和监视器
 - EPOS (电子销售终端)
- 接口
 - USB 2.0/1.1
 - 通用输入/输出 (GPIO)
 - 按钮
 - 音频

3 说明

ESD351 是一种单向 TVS ESD 保护二极管, 具有低动态电阻 R_{DYN} 和低钳位电压。ESD351 的额定 ESD 冲击消散值高达 30kV (接触放电和空气放电), 级别符合 IEC 61000-4-2 标准。超低动态电阻 (0.1 Ω) 和极低钳位电压 (16A TLP 时为 6.5V) 可针对瞬变事件提供系统级保护。该器件的电容为 1.8pF (典型值), 因此非常适用于保护 USB 2.0 等接口。

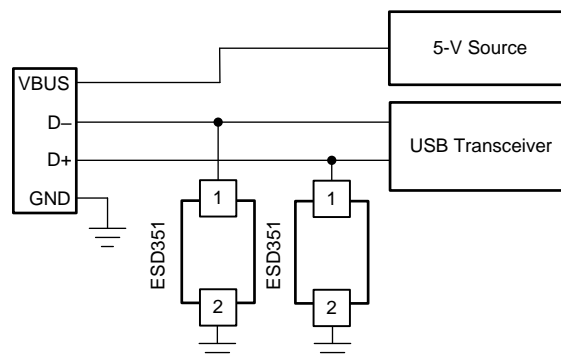
ESD351 采用符合行业标准的 0402 (DPY/DFN1006P2) 封装。

器件信息⁽¹⁾

器件编号	封装	封装尺寸 (标称值)
ESD351	X1SON (2)	0.60mm x 1.00mm

(1) 要了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

典型的 USB 2.0 应用原理图



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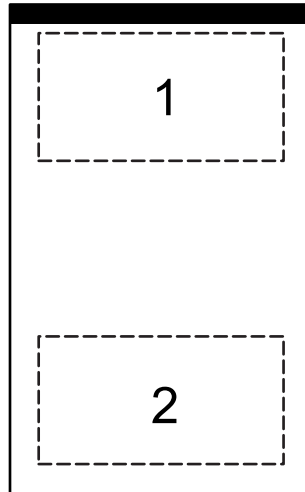
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4 修订历史记录

日期	修订版本	说明
2018 年 7 月	*	初始发行版。

5 Pin Configuration and Functions

DPY Package
2-Pin X1SON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IO	I/O	ESD Protected Channel. Connect this pin to the line being protected.
2	GND	GND	Connect this pin to Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Electrical Fast Transient	IEC 61000-4-4 Peak Current at 25 °C		80	A
Surge Pulse	IEC 61000-4-5 Surge (tp 8/20 μs) Peak Power at 25 °C		36	W
	IEC 61000-4-5 Surge (tp 8/20 μs) Peak Current at 25 °C		6	A
T _A	Operating free-air temperature	–40	125	°C
T _{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings -JEDEC Specifications

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins ⁽¹⁾	±2500
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000
		IEC 61000-4-2 Air Discharge, all pins	±30000

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage	0		3.6	V
T _A	Operating Free Air Temperature	–40		125	°C

6.5 Thermal Information

THERMAL METRIC ⁽¹⁾		ESD351	UNIT
		DPY (X1SON)	
		2 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	409.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	216.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	140.4	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	81.4	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	140.0	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

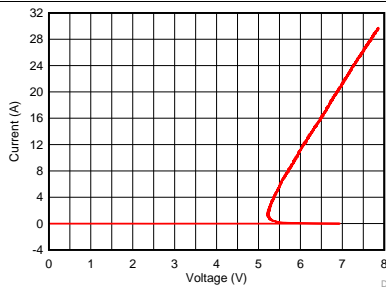
6.6 Electrical Characteristics

At TA = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{RWM}	Reverse stand-off voltage	I _{IO} < 50 nA, across operating temperature range			3.6	V
I _{LEAKAGE}	Leakage current at 3.6 V	V _{IO} = 3.6 V, I/O to GND		0.1	10	nA
V _{BRF}	Breakdown voltage, I/O to GND ⁽¹⁾	I _{IO} = 1 mA	4.5		7.5	V
V _{FWD}	Forward Voltage, GND to I/O ⁽¹⁾	I _{IO} = 1 mA		0.8		V
V _{HOLD}	Holding voltage, I/O to GND ⁽²⁾	I _{IO} = 1 mA		5.1		V
V _{CLAMP}	Clamping voltage	I _{PP} = 6 A (8/20 μs Surge), I/O to GND		6.1		V
		I _{PP} = 16 A (100 ns TLP), I/O to GND		6.5		V
		I _{PP} = 16 A (100 ns TLP), GND to I/O		2.5		V
R _{DYN}	Dynamic resistance	I/O to GND, 100 ns TLP, between 10 to 20 A I _{PP}		0.1		Ω
		GND to I/O, 100 ns TLP, between 10 to 20 A I _{PP}		0.08		
C _{LINE}	Line capacitance, IO to GND	V _{IO} = 0 V, V _{p-p} = 30 mV, f = 1 MHz		1.8	2.2	pF

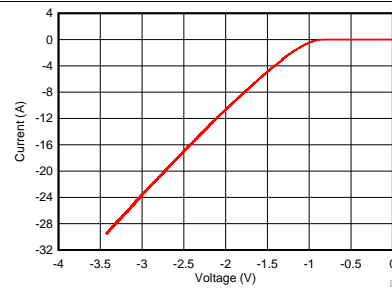
- (1) V_{BRF} and V_{BRR} are defined as the voltage obtained at 1 mA when sweeping the voltage up, before the device latches into the snapback state
- (2) V_{HOLD} is defined as the voltage when 1 mA is applied, after the device has successfully latched into the snapback state.

6.7 Typical Characteristics



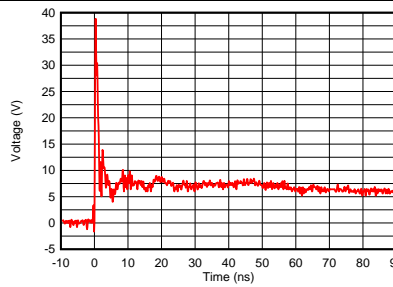
D001_Positive_TLP.grf

图 1. TLP I-V Curve, I/O Pin to GND ($t_p = 100$ ns)



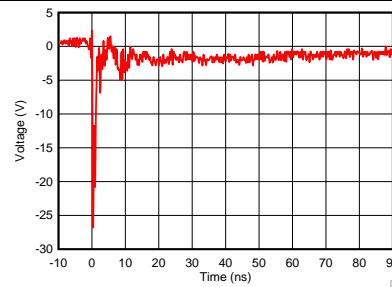
D002_Negative_TLP.grf

图 2. TLP I/V Curve, GND to I/O Pin ($t_p = 100$ ns)



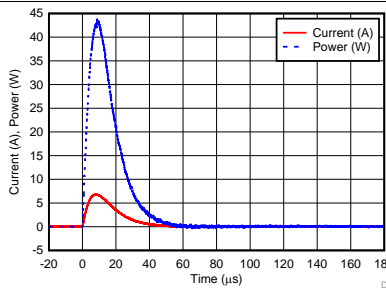
D003_Positive_IEC.grf

图 3. 8-kV IEC 61000-4-2 Clamping Voltage, I/O pin to GND



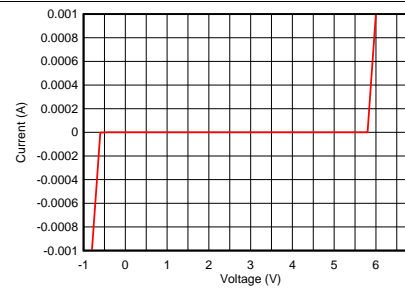
D004_Negative_IEC.grf

图 4. 8-kV IEC 61000-4-2 Clamping Voltage, GND to I/O Pin



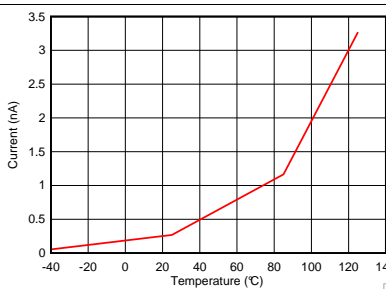
D005_Surge.grf

图 5. Surge Curve (IEC 61000-4-5, $t_p = 8/20$ μ s), I/O Pin to GND



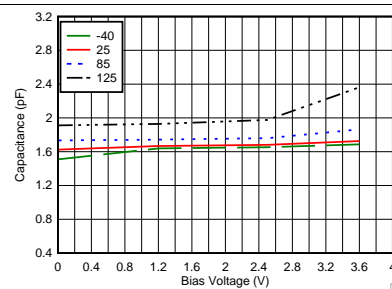
D006_DC.grf

图 6. DC IV-Curve, I/O Pin to GND



D007_Leakage.grf

图 7. Leakage Current at 3.6 V Bias Voltage Across Temperature, I/O Pin to GND



D008_Cap.grf

图 8. Capacitance Vs. Bias Voltage at Different Temperatures ($^{\circ}$ C)

Typical Characteristics (接下页)

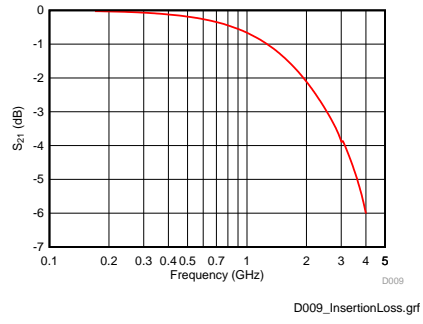


图 9. Insertion Loss Vs. Frequency

7 Detailed Description

7.1 Overview

The ESD351 is a uni-directional ESD Protection Diode with 30 kV IEC 61000-4-2 level (Contact and Air) with ultra-low clamping voltage in a 1 mm × 0.6 mm package. The ultra-low clamping makes this device capable of protecting any ESD-sensitive pins.

7.2 Functional Block Diagram



7.3 Feature Description

ESD351 provides ESD protection up to ± 30 -kV contact and ± 30 -kV air gap per IEC 61000-4-2 standard. During an ESD event, ESD diode connected to the I/O pin turns on and diverts the current to ground. Additionally, ESD351 also provides protection against IEC 61000-4-5 Surge currents up to 6 A (8/20 μ s waveform) and up to 80 A per IEC 61000-4-4 (5/50 ns waveform, 4 kV with 50- Ω impedance) electrical fast transient (EFT) standard. The capacitance between the I/O pin and ground is 1.8 pF (typical) and 2.2 pF (maximum). The device features a low leakage current of 0.1 nA (typical) and 50 nA (maximum, across operating temperature range) with a bias of 3.6 V. The ESD diode at the I/O pin protects the ESD-sensitive devices by clamping the voltage to a low value of 6.5 V ($I_{PP} = 16$ A 100 ns TLP). The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The ESD351 is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{FWD} . During ESD events, voltages as high as ± 30 kV (contact or air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of ESD351 (usually within 10s of nano-seconds) the device reverts to passive.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ESD351 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP} , to a safe level for the protected IC.

8.2 Typical Application

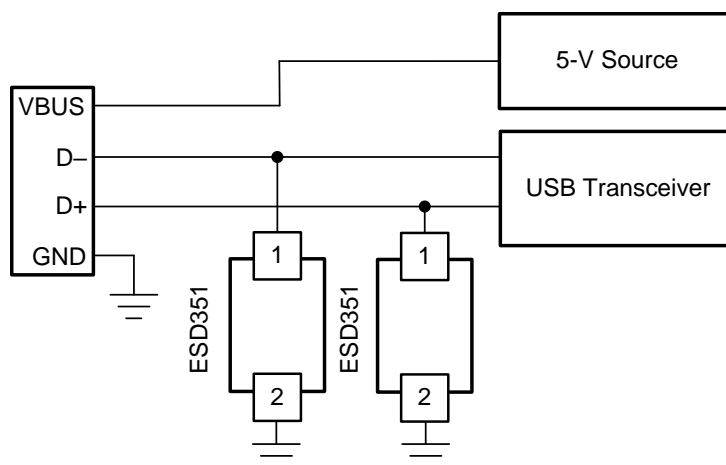


图 10. USB 2.0 ESD Schematic

8.2.1 Design Requirements

For this design example, two ESD351 devices are being used in a USB 2.0 application. This provides a complete ESD protection scheme.

Given the USB 2.0 application, the parameters listed in 表 1 are known.

表 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on DP-DM lines	0 V to 3.6 V
Operating frequency on DP-DM lines	up to 240 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The ESD351 supports signal ranges between 0 V and 3.6 V, which supports the USB 2.0 signal pair on the USB 2.0 application.

8.2.2.2 Operating Frequency

The ESD351 has a 1.8 pF (typical) capacitance, which supports the USB 2.0 data rates of 480 Mbps.

8.2.3 Application Curve

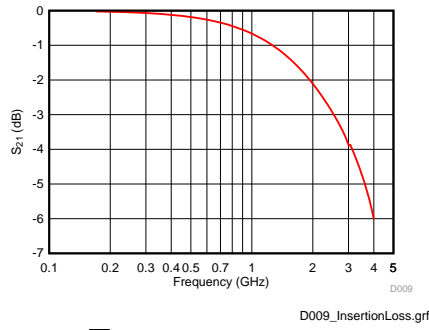


图 11. Insertion Loss

9 Power Supply Recommendations

The ESD351 is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (0 V to 3.6 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
 - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
 - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

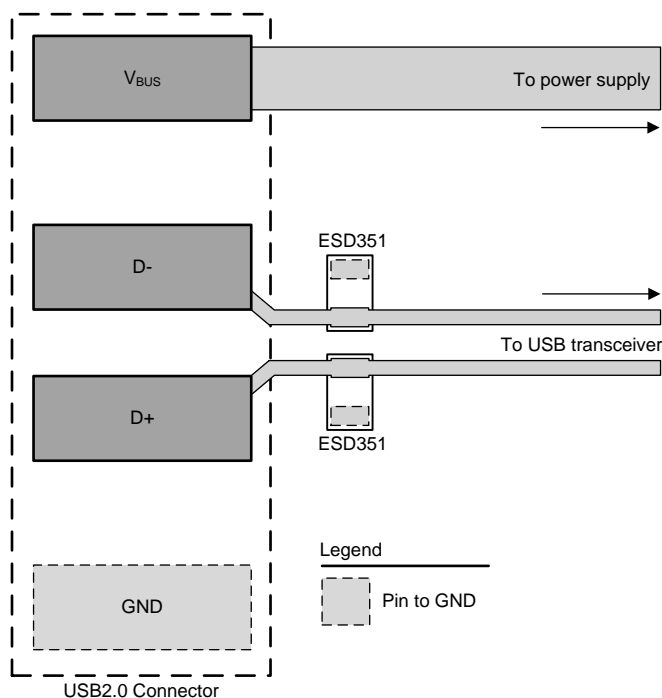


图 12. USB 2.0 ESD Layout

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档:

《通用 ESD 器件评估模块》, [SLVUBG5](#)

11.2 接收文档更新通知

要接收文档更新通知, 请导航至 [TI.com.cn](#) 上的器件产品文件夹。单击右上角的 *通知我* 进行注册, 即可每周接收产品信息更改摘要。有关更改的详细信息, 请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范, 并且不一定反映 TI 的观点; 请参阅 TI 的 [《使用条款》](#)。

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设计支持 *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.4 商标

E2E is a trademark of Texas Instruments.
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11.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序, 可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级, 大至整个器件故障。精密的集成电路可能更容易受到损坏, 这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

[SLYZ022](#) — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更, 恕不另行通知, 且不会对此文档进行修订。如需获取此数据表的浏览器版本, 请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD351DPYR	ACTIVE	X1SON	DPY	2	10000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(A5, DE)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

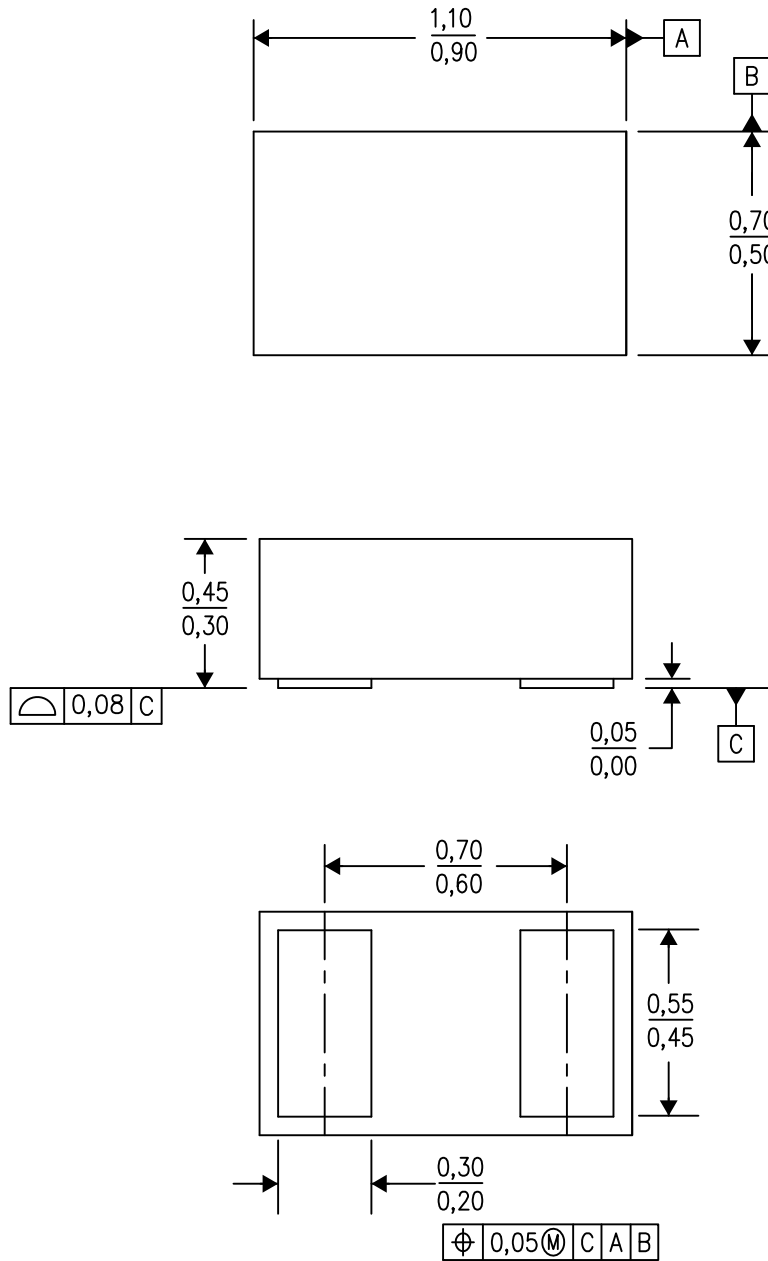
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DPY (R-PX1SON-N2)

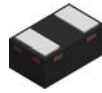
PLASTIC SMALL OUTLINE NO-LEAD



4211012/D 08/14

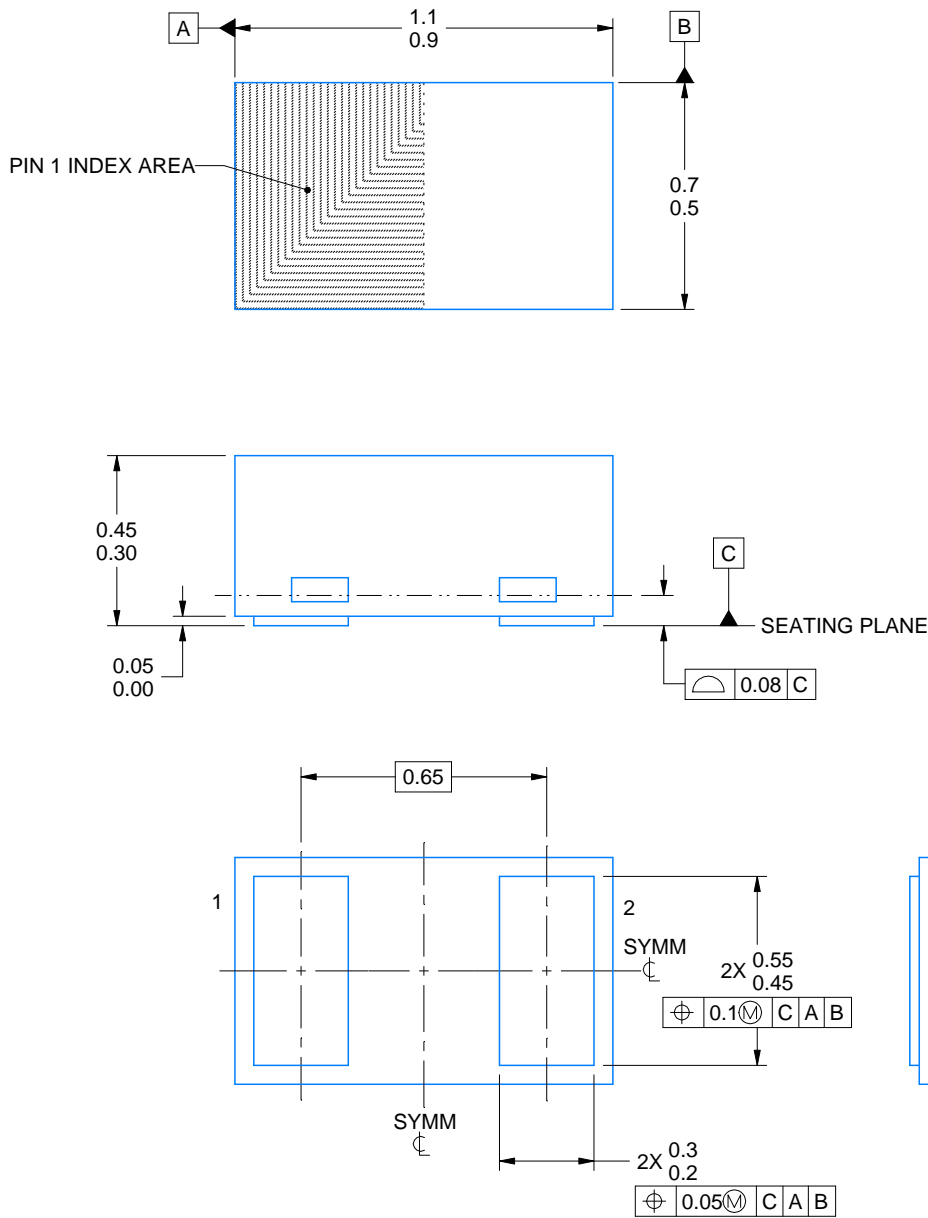
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - This drawing is subject to change without notice.
 - SON (Small Outline No-Lead) package configuration.

DPY0002A



PACKAGE OUTLINE
X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4224561/B 03/2021

NOTES:

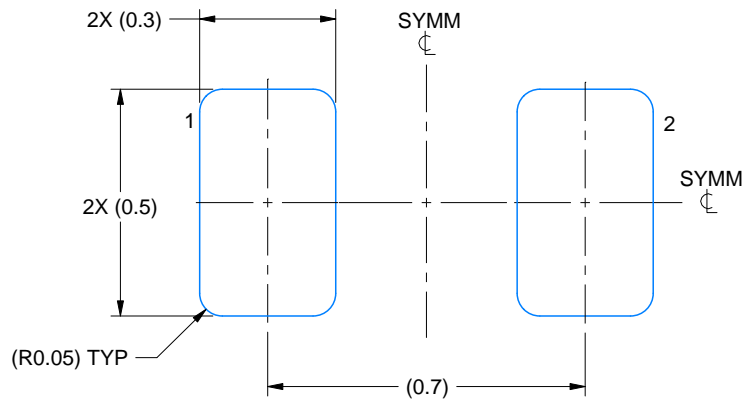
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

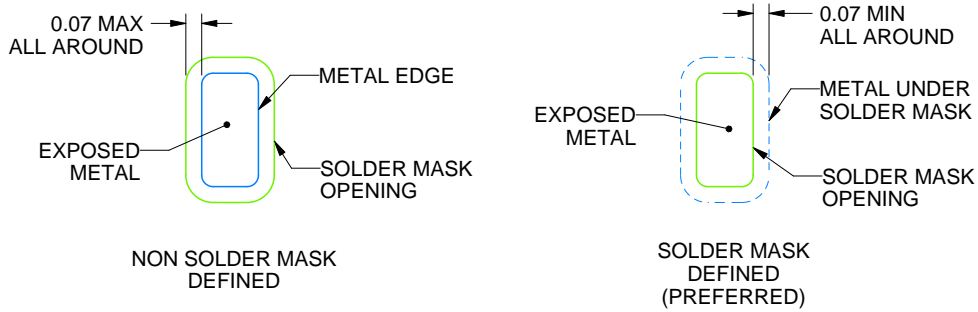
DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS

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NOTES: (continued)

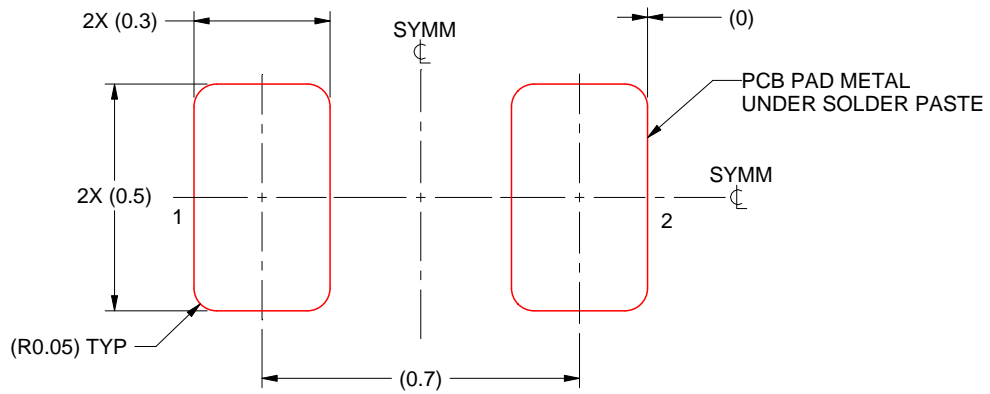
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224561/B 03/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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