Automotive LPDDR SDRAM

MT46H128M16LF – 32 Meg x 16 x 4 Banks
MT46H64M32LF – 16 Meg x 32 x 4 Banks
MT46H128M32L2 – 16 Meg x 32 x 4 Banks x 2
MT46H256M32L4 – 32 Meg x 16 x 4 Banks x 4

Features

- V_{DD}/V_{DDQ} = 1.70–1.95V
- Bidirectional data strobe per byte of data (DQS)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- 4 internal banks for concurrent operation
- Data masks (DM) for masking write data; one mask per byte
- Programmable burst lengths (BL): 2, 4, 8, or 16
- Concurrent auto precharge option is supported
- Auto refresh and self refresh modes
- 1.8V LVCMOS-compatible inputs
- Temperature-compensated self refresh (TCSR)[2]
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- Status read register (SRR)
- Selectable output drive strength (DS)
- Clock stop capability
- 64ms refresh; 32ms for the automotive temperature range

Table 1: Key Timing Parameters (CL = 3)

Speed Grade	Clock Rate	Access Time
-48	208 MHz	4.8ns
-5	200 MHz	5.0ns

Options — Mark

- V_{DD}/V_{DDQ}
  - 1.8V/1.8V — H
- Configuration
  - 256 Meg x 32 (32 Meg x 16 x 4 banks x 4) — 256M32
  - 128 Meg x 32 (16 Meg x 32 x 4 banks x 2) — 128M32
  - 128 Meg x 16 (32 Meg x 16 x 4 banks) — 128M16
  - 64 Meg x 32 (16 Meg x 32 x 4 banks) — 64M32
- Addressing
  - JEDEC-standard — LF
  - 2-die stack standard — L2
  - 4-die stack standard — L4
- Plastic "green" package
  - 60-ball VFBGA (8mm x 9mm) — DD
  - 90-ball VFBGA (8mm x 13mm) — BQ
- PoP (plastic "green" package)
  - 168-ball WFBGA DDP (12mm x 12mm) — KQ
  - 168-ball TFBGA QDP (12mm x 12mm) — SA
- Timing – cycle time
  - 4.8ns @ CL = 3 (208 MHz) — -48
  - 5ns @ CL = 3 (200 MHz) — -5
- Special Options
  - None
  - Automotive (package-level burn-in) — A
- Operating temperature range
  - From –40˚C to +85˚C — IT
  - From –40˚C to +105˚C[1] — AT
  - From –25˚C to +85˚C — WT
- Design revision — :C

Notes: 1. Contact factory for availability.
2. Self refresh supported up to 85 °C.

Table 2: Configuration Addressing – 2Gb

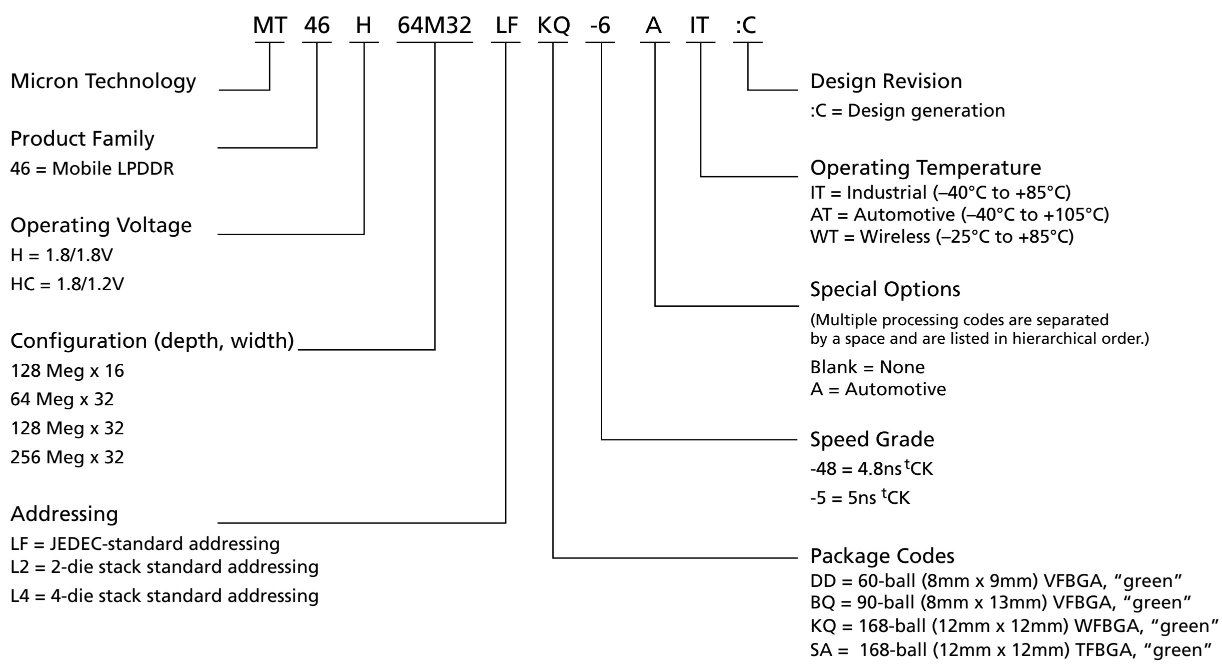
Architecture	128 Meg x 16	64 Meg x 32
Configuration	32 Meg x 16 x 4 banks	16 Meg x 32 x 4 banks

Table 2: Configuration Addressing – 2Gb (Continued)

Architecture	128 Meg x 16	64 Meg x 32
Refresh count	8K	8K
Row addressing	16K A[13:0]	16K A[13:0]
Column addressing	2K A11, A[9:0]	1K A[9:0]

See Package Block Diagrams for descriptions of signal connections and die configurations for each respective architecture.

Figure 1: 2Gb Mobile LPDDR Part Numbering



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

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General Description

The 2Gb Mobile low-power DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 2,147,483,648 bits. It is internally configured as a quad-bank DRAM. Each of the x16's 536,870,912-bit banks is organized as 16,384 rows by 2048 columns by 16 bits. Each of the x32's 536,870,912-bit banks is organized as 16,384 rows by 1024 columns by 32 bits.

Note:

1. Throughout this data sheet, various figures and text refer to DQs as "DQ." DQ should be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into 2 bytes: the lower byte and the upper byte. For the lower byte (DQ[7:0]), DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ[15:8]), DM refers to UDM and DQS refers to UDQS. The x32 is divided into 4 bytes. For DQ[7:0], DM refers to DM0 and DQS refers to DQS0. For DQ[15:8], DM refers to DM1 and DQS refers to DQS1. For DQ[23:16], DM refers to DM2 and DQS refers to DQS2. For DQ[31:24], DM refers to DM3 and DQS refers to DQS3.

2. Complete functionality is described throughout the document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

3. Any specific requirement takes precedence over a general statement.

Functional Block Diagrams

Figure 2: Functional Block Diagram (x16)

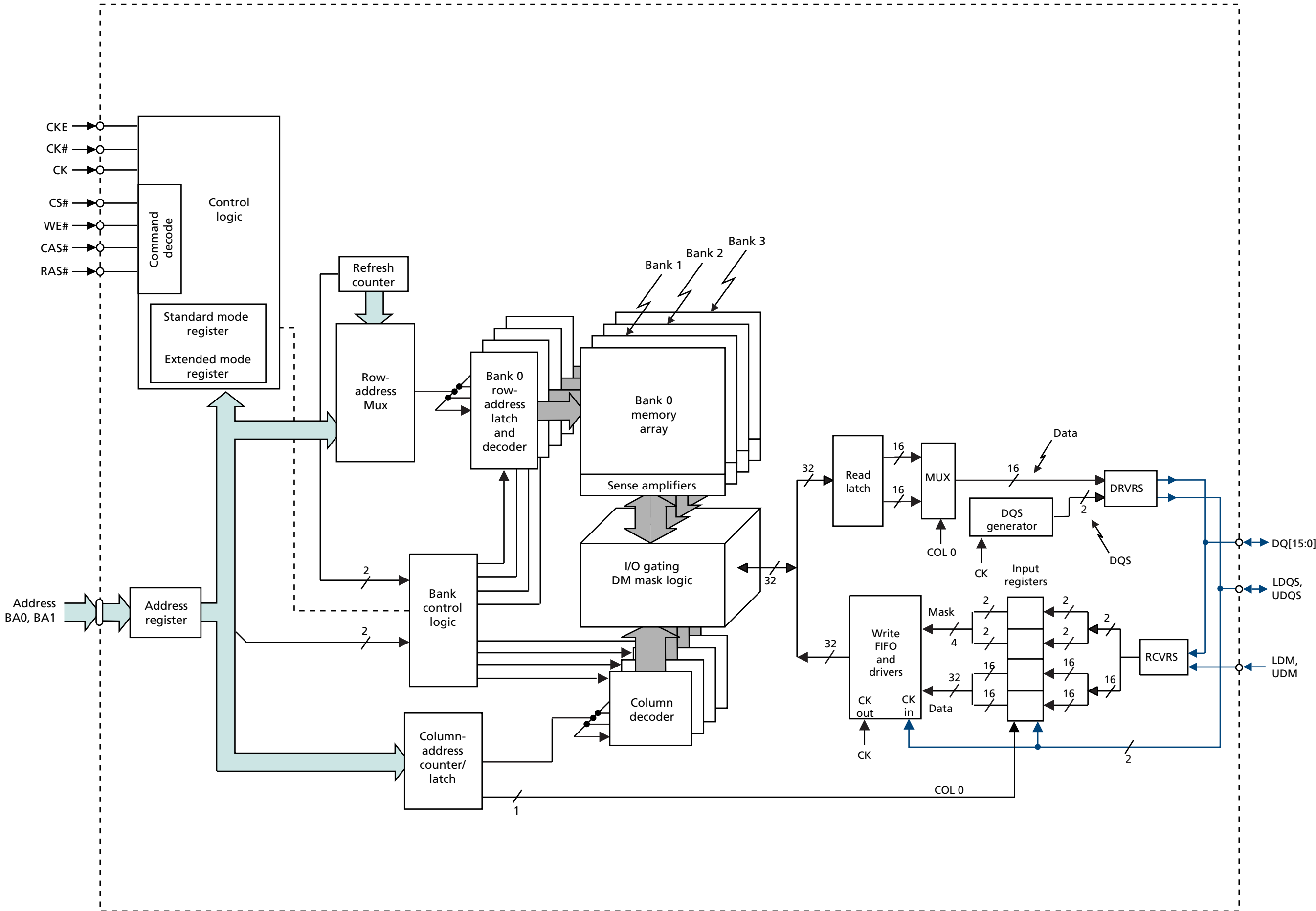
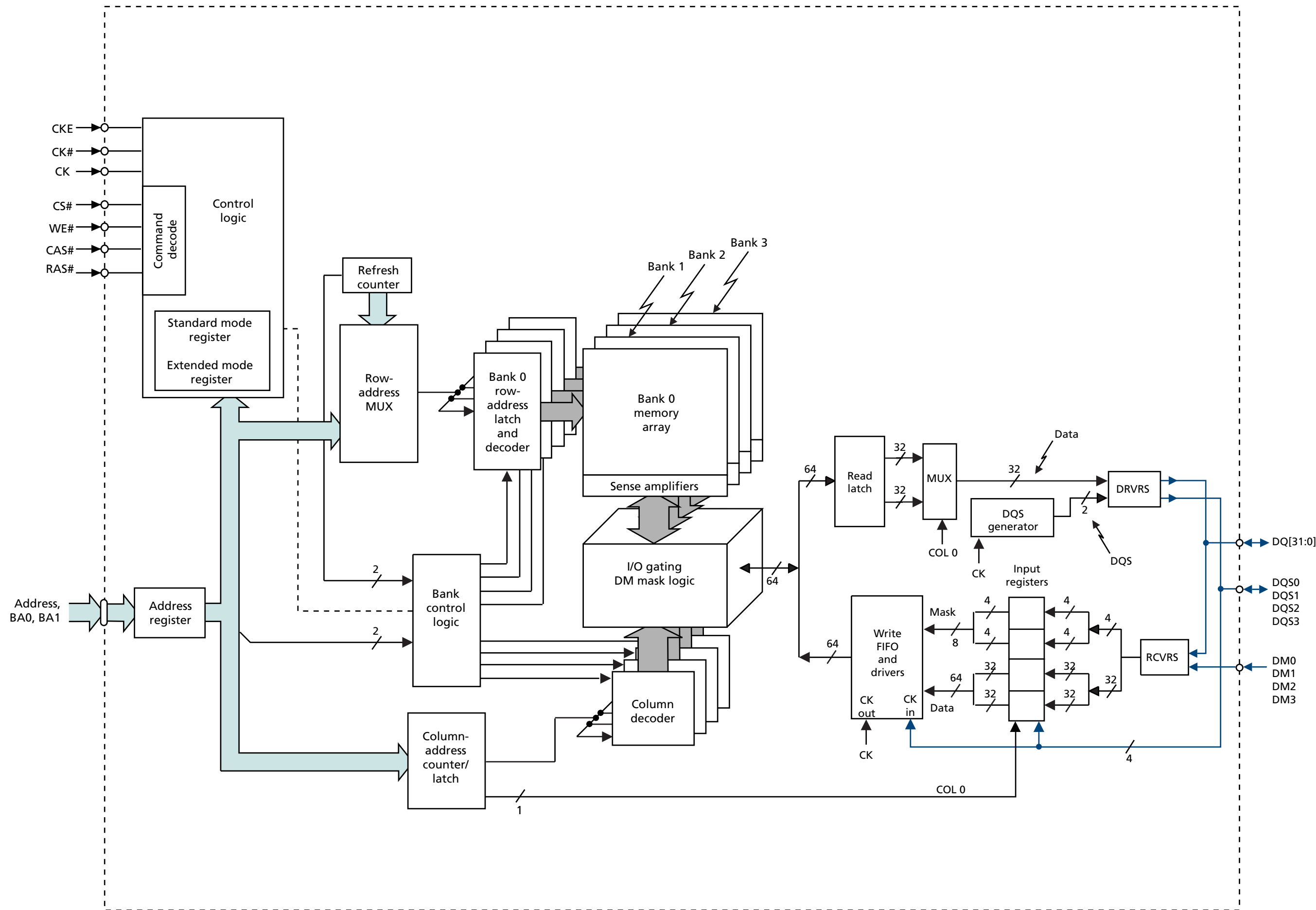


Figure 3: Functional Block Diagram (x32)



Ball Assignments

Figure 4: 60-Ball VFBGA – Top View, x16 only

	1	2	3	4	5	6	7	8	9
A	V_{SS}	DQ15	V_{SSQ}				V_{DDQ}	DQ0	V_{DD}
B	V_{DDQ}	DQ13	DQ14				DQ1	DQ2	V_{SSQ}
C	V_{SSQ}	DQ11	DQ12				DQ3	DQ4	V_{DDQ}
D	V_{DDQ}	DQ9	DQ10				DQ5	DQ6	TEST[1]
E	V_{SSQ}	UDQS	DQ8				DQ7	LDQS	V_{DDQ}
F	V_{SS}	UDM	NC				A13	LDM	V_{DD}
G	CKE	CK	CK#				WE#	CAS#	RAS#
H	A9	A11	A12				CS#	BA0	BA1
J	A6	A7	A8				A10/AP	A0	A1
K	V_{SS}	A4	A5				A2	A3	V_{DD}

Notes:
1. D9 is a test pin that must be tied to V_{SS} or V_{SSQ} in normal operations.
2. Unused address pins become RFU.

Figure 5: 90-Ball VFBGA – Top View, x32 only

	1	2	3	4	5	6	7	8	9
A	V_{SS}	DQ31	V_{SSQ}				V_{DDQ}	DQ16	V_{DD}
B	V_{DDQ}	DQ29	DQ30				DQ17	DQ18	V_{SSQ}
C	V_{SSQ}	DQ27	DQ28				DQ19	DQ20	V_{DDQ}
D	V_{DDQ}	DQ25	DQ26				DQ21	DQ22	TEST[1]
E	V_{SSQ}	DQS3	DQ24				DQ23	DQS2	V_{DDQ}
F	V_{DD}	DM3	NC				A13	DM2	V_{SS}
G	CKE	CK	CK#				WE#	CAS#	RAS#
H	A9	A11	A12				CS#	BA0	BA1
J	A6	A7	A8				A10/AP	A0	A1
K	A4	DM1	A5				A2	DM0	A3
L	V_{SSQ}	DQS1	DQ8				DQ7	DQS0	V_{DDQ}
M	V_{DDQ}	DQ9	DQ10				DQ5	DQ6	V_{SSQ}
N	V_{SSQ}	DQ11	DQ12				DQ3	DQ4	V_{DDQ}
P	V_{DDQ}	DQ13	DQ14				DQ1	DQ2	V_{SSQ}
R	V_{SS}	DQ15	V_{SSQ}				V_{DDQ}	DQ0	V_{DD}

Notes:
1. D9 is a test pin that must be tied to V_{SS} or V_{SSQ} in normal operations.
2. Unused address pins become RFU.

Figure 6: 168-Ball FBGA – 12mm x 12mm (Top View), x32 only

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	DNU	DNU	DQ17	V_{DDQ}	DQ19	DM2	V_{DDQ}	DQ21	DQ23	V_{DDQ}	CK	V_{DD}	DQ9	DQ11	V_{DDQ}	DQ13	DM1	V_{DDQ}	DQ15	DM3	DQ25	DNU	DNU	A
B	DNU	DNU	DQ16	V_{SSQ}	DQ18	DQS2	V_{SSQ}	DQ20	DQ22	V_{SSQ}	CK#	V_{SS}	DQ8	DQ10	V_{SSQ}	DQ12	DQS1	V_{SSQ}	DQ14	DQS3	DQ24	DNU	DNU	B
C	DM0	DQS0																				V_{SSQ}	V_{DDQ}	C
D	DQ7	DQ6																				DQ26	DQ27	D
E	V_{DDQ}	V_{SSQ}																				DQ28	DQ29	E
F	DQ5	DQ4																				V_{SSQ}	V_{DDQ}	F
G	DQ3	DQ2																				DQ30	DQ31	G
H	V_{DDQ}	V_{SSQ}																				V_{SS}	V_{DD}	H
J	DQ1	DQ0																				CKE0	CKE1	J
K	V_{DD}	V_{SS}																				V_{SS}	WE#	K
L	NC[1]	V_{SS}																				CAS#	RAS#	L
M	NC	NC																				CS0#	CS1#	M
N	NC	NC																				A0	A1	N
P	NC[1]	V_{SS}																				A2	A3	P
R	NC	NC																				A4	A5	R
T	NC	NC																				A6	A7	T
U	NC[1]	V_{SS}																				A8	A9	U
V	NC	NC																				A10	A11	V
W	NC	NC																				A12	A13	W
Y	NC	NC																				A14	V_{DD}	Y
AA	NC[1]	V_{SS}																				V_{SS}	V_{DD}	AA
AB	DNU	DNU	NC	NC	V_{SS}	NC	NC	V_{SS}	NC	NC	NC	NC	V_{SS}	V_{SS}	NC	NC	NC	NC	NC	V_{SS}	BA0	DNU	DNU	AB
AC	DNU	DNU	NC	NC	NC[1]	NC	NC	NC[1]	NC	NC	NC	NC	NC[1]	TQ	NC	NC	NC	NC	NC	NC	BA1	DNU	DNU	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

Top View – Ball Down

LPDDR Supply Ground

Note: 1. Although not bonded to the die, these pins may be connected on the package substrate.

Ball Descriptions

The ball descriptions table is a comprehensive list of all possible balls for all supported packages. Not all balls listed are supported for a given package.

Table 3: Ball Descriptions

Symbol	Type	Description
CK, CK#	Input	Clock: CK is the system clock input. CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Input and output data is referenced to the crossing of CK and CK# (both directions of the crossing).
CKE CKE0, CKE1	Input	Clock enable: CKE HIGH activates, and CKE LOW deactivates, the internal clock signals, input buffers, and output drivers. Taking CKE LOW enables PRECHARGE power-down and SELF REFRESH operations (all banks idle), or ACTIVE power-down (row active in any bank). CKE is synchronous for all functions except SELF REFRESH exit. All input buffers (except CKE) are disabled during power-down and self refresh modes. CKE0 is used for a single LPDDR product. CKE1 is used for dual LPDDR products and is considered RFU for single LPDDR MCPs.
CS# CS0#, CS1#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code. CS0# is used for a single LPDDR product. CS1# is used for dual LPDDR products and is considered RFU for single LPDDR MCPs.
RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
UDM, LDM (x16) DM[3:0] (x32)	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls.
BA0, BA1	Input	Bank address inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register is loaded during a LOAD MODE REGISTER command.
A[13:0]	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ or WRITE commands, to select one location out of the memory array in the respective bank. During a PRECHARGE command, A10 determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command. The maximum address range is dependent upon configuration. Unused address balls become RFU.
TEST	Input	Test pin: Must be tied to V_{SS} or V_{SSQ} in normal operations.
DQ[15:0] (x16) DQ[31:0] (x32)	Input/ output	Data input/output: Data bus for x16 and x32.
LDQS, UDQS (x16) DQS[3:0] (x32)	Input/ output	Data strobe: Output with read data, input with write data. DQS is edge-aligned with read data, center-aligned in write data. It is used to capture data.
TQ	Output	Temperature sensor output: TQ HIGH when LPDDR T_J exceeds 85°C.
V_{DDQ}	Supply	DQ power supply.

Table 3: Ball Descriptions (Continued)

Symbol	Type	Description
V_{SSQ}	Supply	DQ ground.
V_{DD}	Supply	Power supply.
V_{SS}	Supply	Ground.
NC	–	No connect: May be left unconnected.
RFU	–	Reserved for future use. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

Package Block Diagrams

Figure 7: Single Rank, Single Channel (1 Die) Package Block Diagram

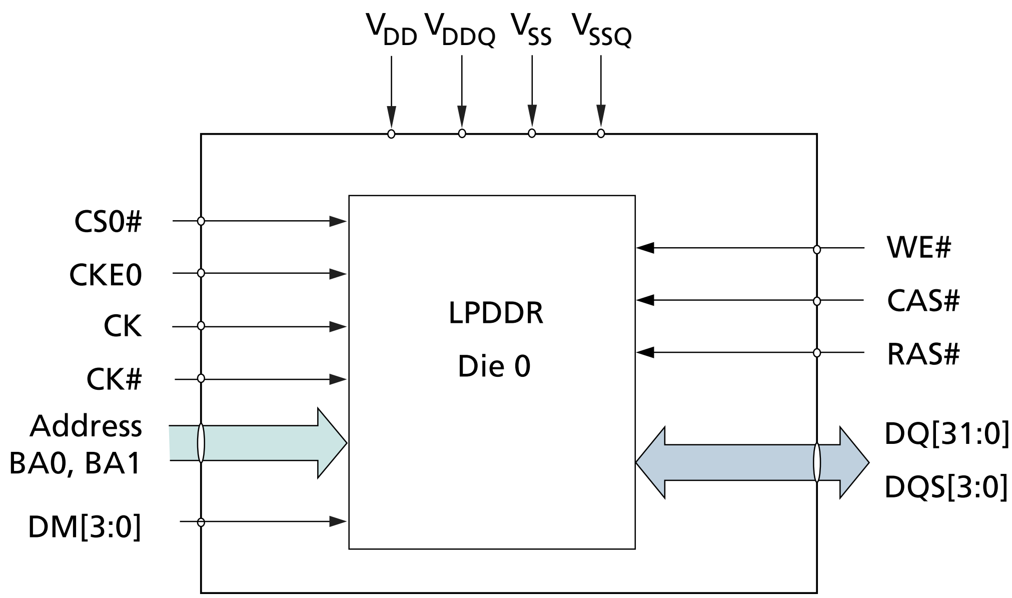


Figure 8: Dual Rank, Single Channel (2 Die) Package Block Diagram

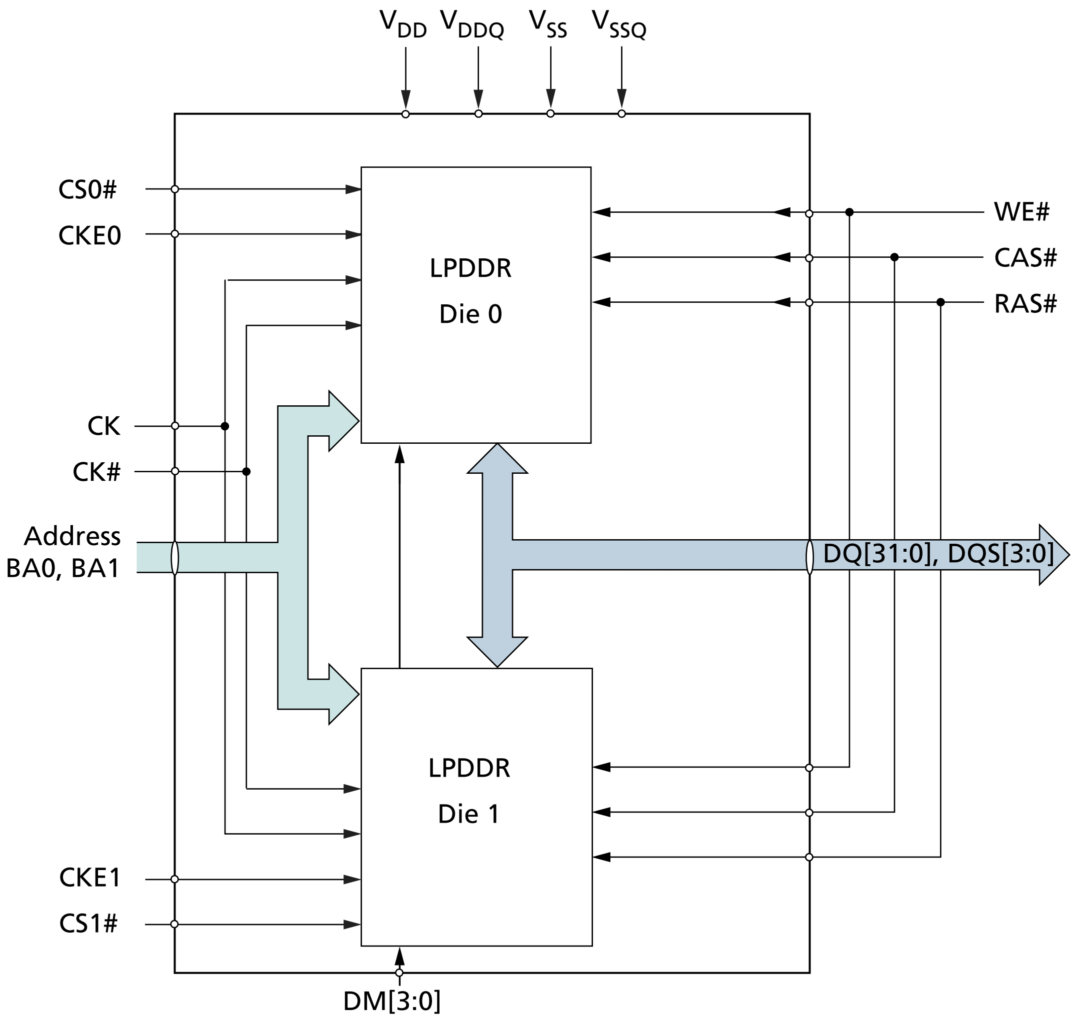
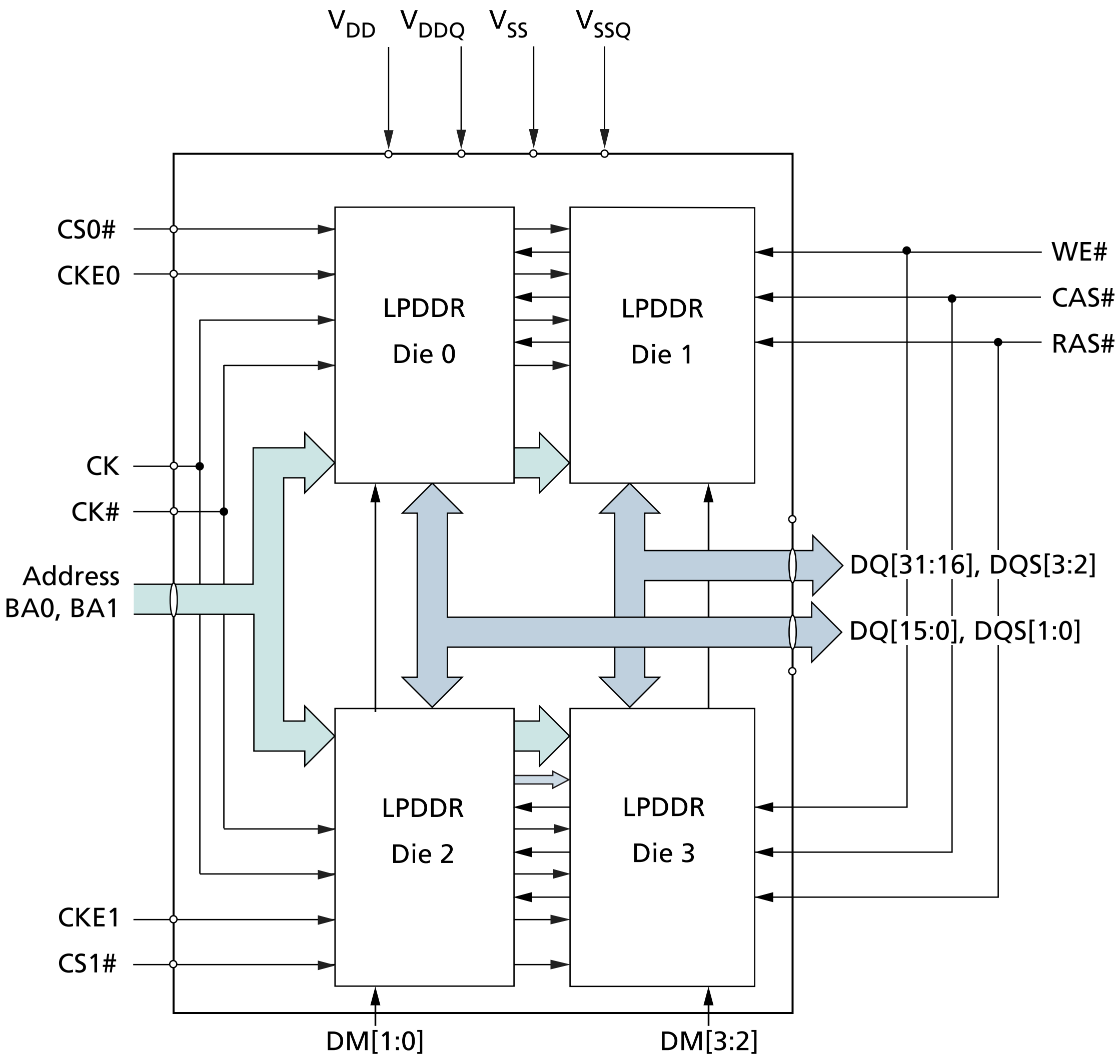
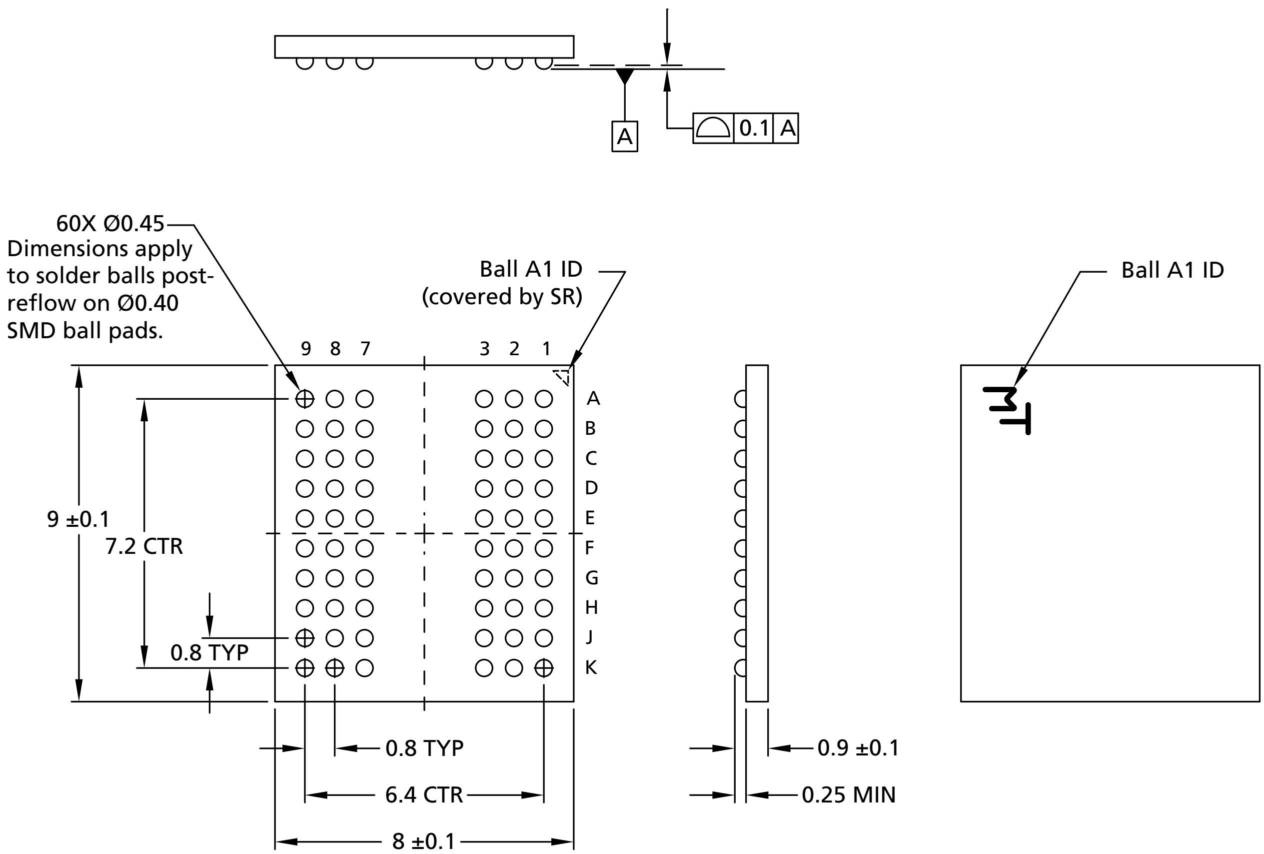


Figure 9: Dual Rank, Single Channel (4 Die) Package Block Diagram



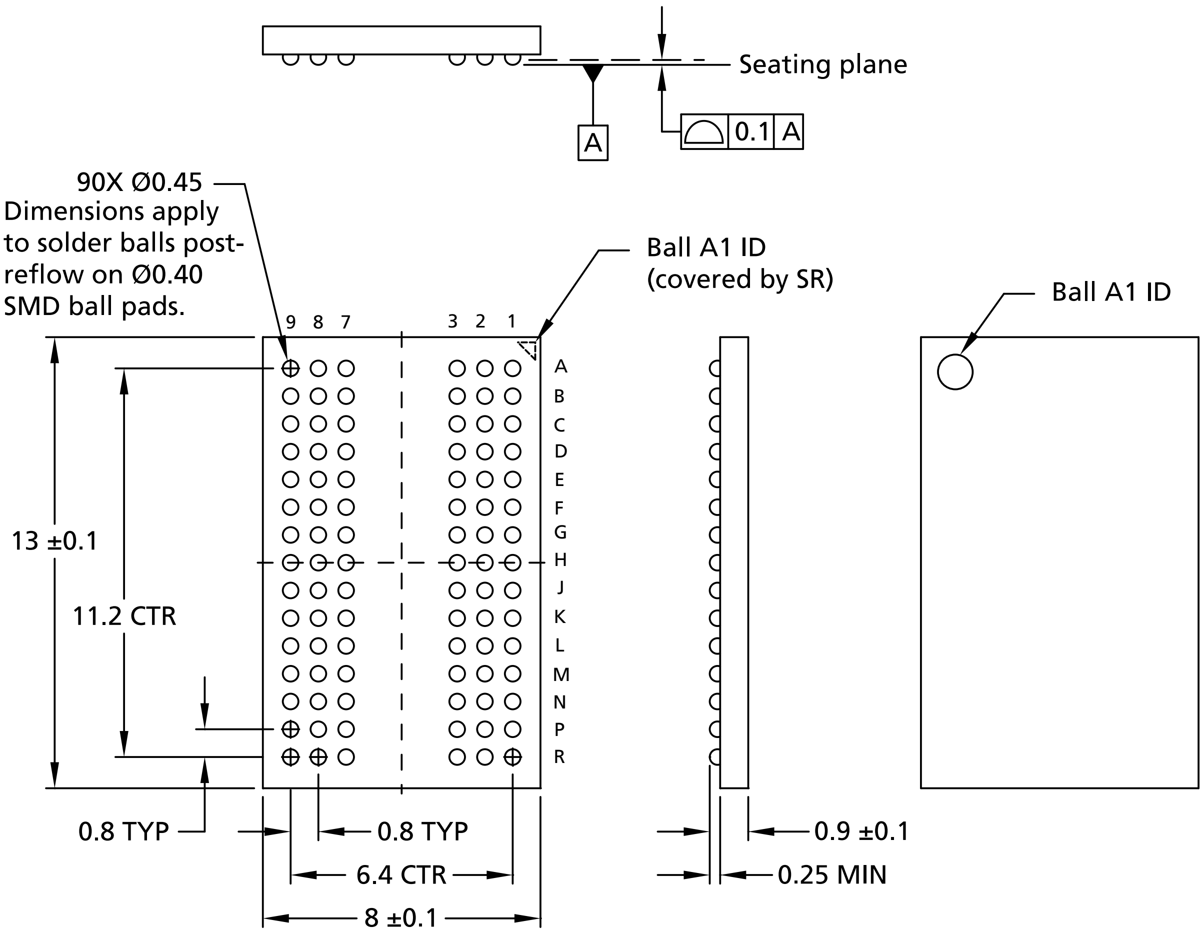
Package Dimensions

Figure 10: 60-Ball VFBGA (8mm x 9mm), Package Code: DD



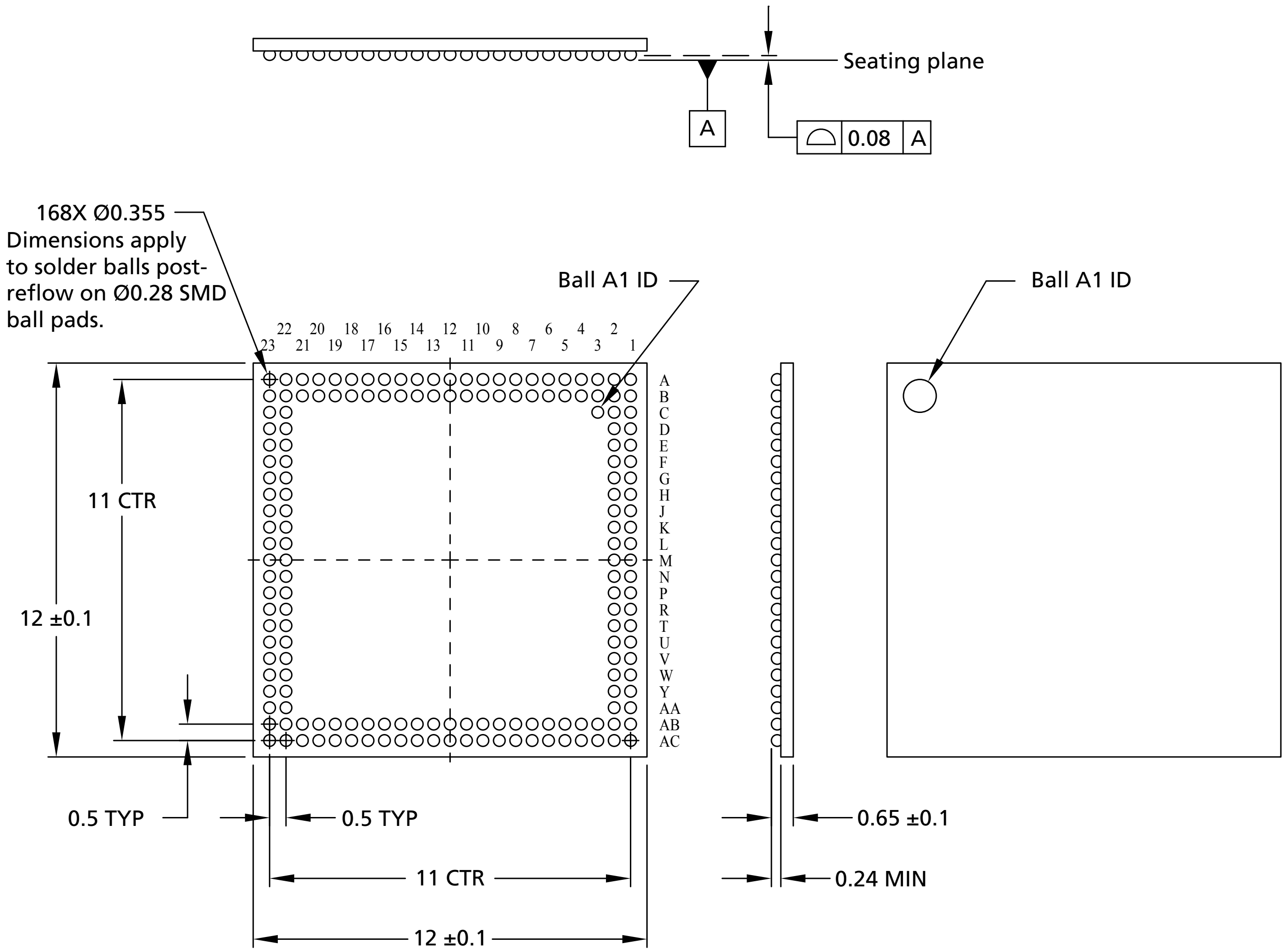
Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Figure 11: 90-Ball VFBGA (8mm x 13mm), Package Code: BQ



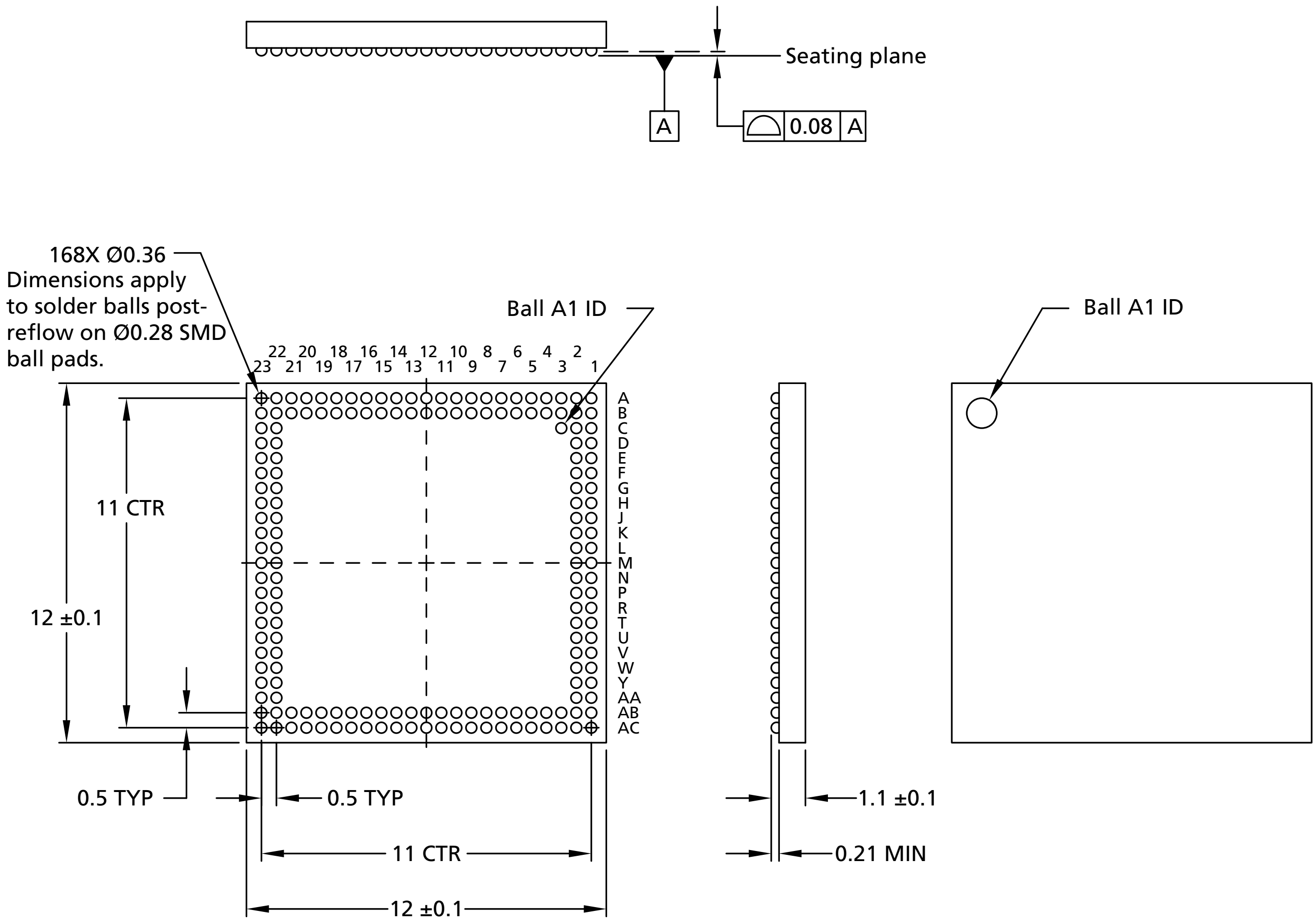
Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Figure 12: 168-Ball FBGA (12mm x 12mm), Package Code: KQ



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC105 (98.5% Sn, 1% Ag, 0.5% Cu).

Figure 13: 168-Ball FBGA (12mm x 12mm), Package Code: SA



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC105 (98.5% Sn, 1% Ag, 0.5% Cu).

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 4: Absolute Maximum Ratings

Note 1 applies to all parameters in this table

Parameter	Symbol	Min	Max	Unit
V_{DD}/V_{DDQ} supply voltage relative to V_{SS}	V_{DD}/V_{DDQ}	–1.0	2.4	V
Voltage on any pin relative to V_{SS}	V_{IN}	–0.5	2.4 or (V_{DDQ} + 0.3V), whichever is less	V
Storage temperature (plastic)	T_{STG}	–55	150	˚C

Note: 1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times. V_{DDQ} must not exceed V_{DD}.

Table 5: AC/DC Electrical Characteristics and Operating Conditions

Notes 1–5 apply to all parameters/conditions in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

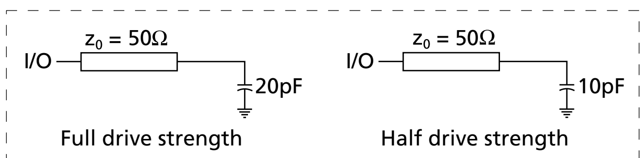
Parameter/Condition	Symbol	Min	Max	Unit	Notes
Supply voltage	V_{DD}	1.70	1.95	V	6, 7
I/O supply voltage	V_{DDQ}	1.70	1.95	V	6, 7
Address and command inputs					
Input voltage high	V_{IH}	0.8 × V_{DDQ}	V_{DDQ} + 0.3	V	8, 9
Input voltage low	V_{IL}	–0.3	0.2 × V_{DDQ}	V	8, 9
Clock inputs (CK, CK#)					
DC input voltage	V_{IN}	–0.3	V_{DDQ} + 0.3	V	10
DC input differential voltage	$V_{ID(DC)}$	0.4 × V_{DDQ}	V_{DDQ} + 0.6	V	10, 11
AC input differential voltage	$V_{ID(AC)}$	0.6 × V_{DDQ}	V_{DDQ} + 0.6	V	10, 11
AC differential crossing voltage	V_{IX}	0.4 × V_{DDQ}	0.6 × V_{DDQ}	V	10, 12
Data inputs					
DC input high voltage	$V_{IH(DC)}$	0.7 × V_{DDQ}	V_{DDQ} + 0.3	V	8, 9, 13
DC input low voltage	$V_{IL(DC)}$	–0.3	0.3 × V_{DDQ}	V	8, 9, 13
AC input high voltage	$V_{IH(AC)}$	0.8 × V_{DDQ}	V_{DDQ} + 0.3	V	8, 9, 13
AC input low voltage	$V_{IL(AC)}$	–0.3	0.2 × V_{DDQ}	V	8, 9, 13
Data outputs					
DC output high voltage: Logic 1 (I_{OH} = –0.1mA)	V_{OH}	0.9 × V_{DDQ}	–	V	
DC output low voltage: Logic 0 (I_{OL} = 0.1mA)	V_{OL}	–	0.1 × V_{DDQ}	V	
Leakage current					
Input leakage current Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	I_I	–1	1	µA	

Table 5: AC/DC Electrical Characteristics and Operating Conditions (Continued)

Notes 1–5 apply to all parameters/conditions in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output leakage current (DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})	I_{OZ}	–1.5	1.5	µA	
Operating temperature					
Commercial	T_A	0	70	˚C	
Wireless	T_A	–25	85	˚C	
Industrial	T_A	–40	85	˚C	
Automotive	T_A	–40	105	˚C	

Notes:
1. All voltages referenced to V_{SS}.
2. All parameters assume proper device initialization.
3. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
4. Outputs measured with equivalent load; transmission line delay is assumed to be very small:



5. Timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to $V_{DDQ/2}$ (or to the crossing point for CK/CK#). The output timing reference voltage level is $V_{DDQ/2}$.
6. Any positive glitch must be less than one-third of the clock cycle and not more than +200mV or 2.0V, whichever is less. Any negative glitch must be less than one-third of the clock cycle and not exceed either –150mV or +1.6V, whichever is more positive.
7. V_{DD} and V_{DDQ} must track each other and V_{DDQ} must be less than or equal to V_{DD}.
8. To maintain a valid level, the transitioning edge of the input must:
   8a. Sustain a constant slew rate from the current AC level through to the target AC level, $V_{IL(AC)}$ Or $V_{IH(AC)}$.
   8b. Reach at least the target AC level.
   8c. After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL(DC)}$ or $V_{IH(DC)}$.
9. V_{IH} overshoot: V_{IHmax} = V_{DDQ} + 1.0V for a pulse width ≤3ns and the pulse width cannot be greater than one-third of the cycle rate. V_{IL} undershoot: V_{ILmin} = –1.0V for a pulse width ≤3ns and the pulse width cannot be greater than one-third of the cycle rate.
10. CK and CK# input slew rate must be ≥1 V/ns (2 V/ns if measured differentially).
11. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
12. The value of V_{IX} is expected to equal $V_{DDQ/2}$ of the transmitting device and must track variations in the DC level of the same.
13. DQ and DM input slew rates must not deviate from DQS by more than 10%. 50ps must be added to ^tDS and ^tDH for each 100 mV/ns reduction in slew rate. If slew rate exceeds 4 V/ns, functionality is uncertain.

Table 6: Capacitance (x16, x32)

Notes 1 and 2 apply to all the parameters in this table

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance: CK, CK#	C_{CK}	1.0	2.0	pF	
Delta input capacitance: CK, CK#	C_{DCK}	0	0.25	pF	3
Input capacitance: command and address	C_I	1.0	2.0	pF	
Delta input capacitance: command and address	C_{DI}	– 0.5	0.5	pF	3
Input/output capacitance: DQ, DQS, DM	C_{IO}	1.25	2.5	pF	
Delta input/output capacitance: DQ, DQS, DM	C_{DIO}	– 0.6	0.6	pF	4

Notes:
1. This parameter is sampled. V_{DD}/V_{DDQ} = 1.70–1.95V, f = 100 MHz, T_A = 25°C, $V_{OUT(DC)}$ = $V_{DDQ}/2$, V_{OUT} (peak-to-peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
2. This parameter applies to die devices only (does not include package capacitance).
3. The input capacitance per pin group will not differ by more than this maximum amount for any given device.
4. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.

Electrical Specifications – I_{DD} Parameters

Table 7: I_{DD} Specifications and Conditions, –40°C to +85°C (x16)

Notes 1–5 apply to all the parameters/conditions in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition		Symbol	Max -48	Max -5	Unit	Notes
Operating 1 bank active precharge current: $^tRC = {^tRC}$ (MIN); $^tCK = {^tCK}$ (MIN); CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every 2 clock cycles; Data bus inputs are stable		I_{DD0}	75	75	mA	6
Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH; $^tCK = {^tCK}$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD2P}	900	900	µA	7, 8
Precharge power-down standby current: Clock stopped; All banks idle; CKE is LOW; CS is HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD2PS}	900	900	µA	7
Precharge nonpower-down standby current: All banks idle; CKE = HIGH; CS = HIGH; $^tCK = {^tCK}$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD2N}	15	15	mA	9
Precharge nonpower-down standby current: Clock stopped; All banks idle; CKE = HIGH; CS = HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD2NS}	9	9	mA	9
Active power-down standby current: 1 bank active; CKE = LOW; CS = HIGH; $^tCK = {^tCK}$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD3P}	5	5	mA	8
Active power-down standby current: Clock stopped; 1 bank active; CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD3PS}	5	5	mA	
Active nonpower-down standby: 1 bank active; CKE = HIGH; CS = HIGH; $^tCK = {^tCK}$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD3N}	17	17	mA	6
Active nonpower-down standby: Clock stopped; 1 bank active; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD3NS}	14	14	mA	6
Operating burst read: 1 bank active; BL = 4; $^tCK = {^tCK}$ (MIN); Continuous READ bursts; Iout = 0mA; Address inputs are switching every 2 clock cycles; 50% data changing each burst		I_{DD4R}	90	90	mA	6
Operating burst write: 1 bank active; BL = 4; $^tCK = {^tCK}$ (MIN); Continuous WRITE bursts; Address inputs are switching; 50% data changing each burst		I_{DD4W}	90	90	mA	6
Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable	^tRFC = 138ns	I_{DD5}	170	170	mA	10
	$^tRFC = {^tREFI}$	I_{DD5A}	12	12	mA	10, 11
Deep power-down current: Address and control balls are stable; Data bus inputs are stable		I_{DD8}	10	10	µA	7, 13

Table 8: I_{DD} Specifications and Conditions, –40°C to +85°C (x32)

Notes 1–5 apply to all the parameters/conditions in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition		Symbol	Max		Unit	Notes
			-48	-5		
Operating 1 bank active precharge current: $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every 2 clock cycles; Data bus inputs are stable		I_{DD0}	75	75	mA	6
Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD2P}	900	900	µA	7, 8
Precharge power-down standby current: Clock stopped; All banks idle; CKE is LOW; CS is HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD2PS}	900	900	µA	7
Precharge nonpower-down standby current: All banks idle; CKE = HIGH; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD2N}	15	15	mA	9
Precharge nonpower-down standby current: Clock stopped; All banks idle; CKE = HIGH; CS = HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD2NS}	9	9	mA	9
Active power-down standby current: 1 bank active; CKE = LOW; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD3P}	5	5	mA	8
Active power-down standby current: Clock stopped; 1 bank active; CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD3PS}	5	5	mA	
Active nonpower-down standby: 1 bank active; CKE = HIGH; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD3N}	17	17	mA	6
Active nonpower-down standby: Clock stopped; 1 bank active; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD3NS}	14	14	mA	6
Operating burst read: 1 bank active; BL = 4; $^tCK = {}^tCK$ (MIN); Continuous READ bursts; Iout = 0mA; Address inputs are switching every 2 clock cycles; 50% data changing each burst		I_{DD4R}	90	90	mA	6
Operating burst write: 1 bank active; BL = 4; $^tCK = {}^tCK$ (MIN); Continuous WRITE bursts; Address inputs are switching; 50% data changing each burst		I_{DD4W}	90	90	mA	6
Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable	^tRFC = 138ns	I_{DD5}	170	170	mA	10
	$^tRFC = {}^tREFI$	I_{DD5A}	12	12	mA	10, 11
Deep power-down current: Address and control balls are stable; Data bus inputs are stable		I_{DD8}	10	10	µA	7, 13

Table 9: I_{DD} Specifications and Conditions, –40°C to +105°C (x16)

Notes 1–5 apply to all the parameters/conditions in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition		Symbol	Max -48	Max -5	Unit	Notes
Operating 1 bank active precharge current: $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every 2 clock cycles; Data bus inputs are stable		I_{DD0}	100	100	mA	6
Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD2P}	1500	1500	μA	7, 8
Precharge power-down standby current: Clock stopped; All banks idle; CKE is LOW; CS is HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD2PS}	1500	1500	μA	7
Precharge nonpower-down standby current: All banks idle; CKE = HIGH; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD2N}	19	19	mA	9
Precharge nonpower-down standby current: Clock stopped; All banks idle; CKE = HIGH; CS = HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD2NS}	13	13	mA	9
Active power-down standby current: 1 bank active; CKE = LOW; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD3P}	9	9	mA	8
Active power-down standby current: Clock stopped; 1 bank active; CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD3PS}	9	9	mA	
Active nonpower-down standby: 1 bank active; CKE = HIGH; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD3N}	21	21	mA	6
Active nonpower-down standby: Clock stopped; 1 bank active; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD3NS}	18	18	mA	6
Operating burst read: 1 bank active; BL = 4; $^tCK = {}^tCK$ (MIN); Continuous READ bursts; Iout = 0mA; Address inputs are switching every 2 clock cycles; 50% data changing each burst		I_{DD4R}	130	130	mA	6
Operating burst write: 1 bank active; BL = 4; $^tCK = {}^tCK$ (MIN); Continuous WRITE bursts; Address inputs are switching; 50% data changing each burst		I_{DD4W}	130	130	mA	6
Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable	^tRFC = 138ns	I_{DD5}	170	170	mA	10
	$^tRFC = {}^tREFI$	I_{DD5A}	13	13	mA	10, 11
Deep power-down current: Address and control balls are stable; Data bus inputs are stable		I_{DD8}	15	15	μA	7, 13

Table 10: I_{DD} Specifications and Conditions, –40°C to +105°C (x32)

Notes 1–5 apply to all the parameters/conditions in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition		Symbol	Max -48	Max -5	Unit	Notes
Operating 1 bank active precharge current: $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every 2 clock cycles; Data bus inputs are stable		I_{DD0}	100	100	mA	6
Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD2P}	1500	1500	μA	7, 8
Precharge power-down standby current: Clock stopped; All banks idle; CKE is LOW; CS is HIGH, CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD2PS}	1500	1500	μA	7
Precharge nonpower-down standby current: All banks idle; CKE = HIGH; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD2N}	19	19	mA	9
Precharge nonpower-down standby current: Clock stopped; All banks idle; CKE = HIGH; CS = HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD2NS}	13	13	mA	9
Active power-down standby current: 1 bank active; CKE = LOW; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD3P}	9	9	mA	8
Active power-down standby current: Clock stopped; 1 bank active; CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD3PS}	9	9	mA	
Active nonpower-down standby: 1 bank active; CKE = HIGH; CS = HIGH; $^tCK = {}^tCK$ (MIN); Address and control inputs are switching; Data bus inputs are stable		I_{DD3N}	21	21	mA	6
Active nonpower-down standby: Clock stopped; 1 bank active; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD3NS}	18	18	mA	6
Operating burst read: 1 bank active; BL = 4; CL = 3; $^tCK = {}^tCK$ (MIN); Continuous READ bursts; Iout = 0mA; Address inputs are switching every 2 clock cycles; 50% data changing each burst		I_{DD4R}	150	150	mA	6
Operating burst write: One bank active; BL = 4; $^tCK = {}^tCK$ (MIN); Continuous WRITE bursts; Address inputs are switching; 50% data changing each burst		I_{DD4W}	150	150	mA	6
Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable	^tRFC = 138ns	I_{DD5}	170	170	mA	10
	$^tRFC = {}^tREFI$	I_{DD5A}	13	13	mA	10, 11
Deep power-down current: Address and control pins are stable; Data bus inputs are stable		I_{DD8}	15	15	μA	7, 13

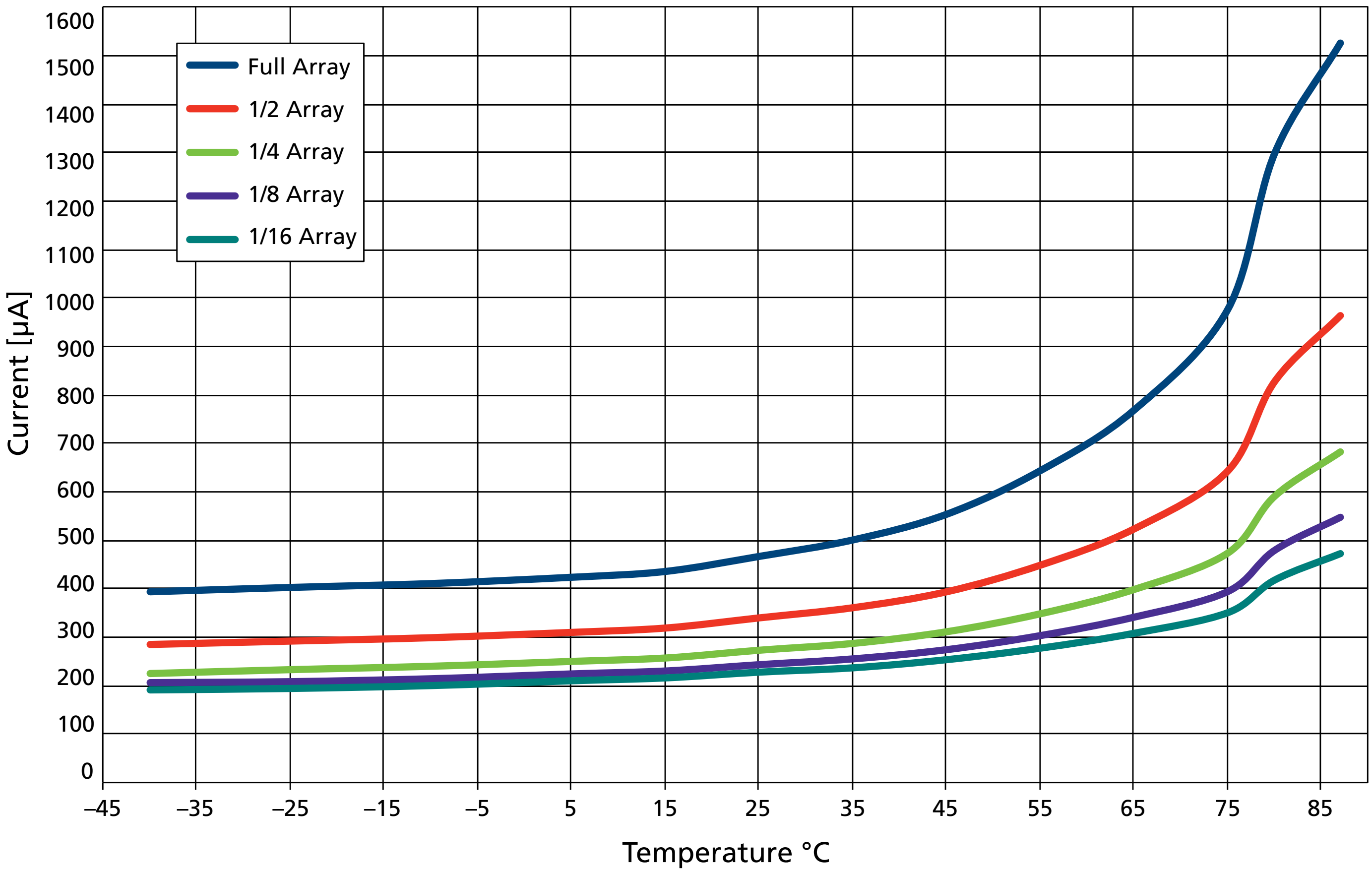
Table 11: $I_{DD}6$ Specifications and Conditions

Notes 1–5, 7, and 12 apply to all the parameters/conditions in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition		Symbol	Value	Units
Self refresh: CKE = LOW; $^{t}CK = {}^{t}CK$ (MIN); Address and control inputs are stable; Data bus inputs are stable	Full array, 105˚C	I_{DD6}	n/a[14]	µA
	Full array, 85˚C		2000	µA
	Full array, 45˚C		900	µA
	1/2 array, 85˚C		1450	µA
	1/2 array, 45˚C		700	µA
	1/4 array, 85˚C		1230	µA
	1/4 array, 45˚C		600	µA
	1/8 array, 85˚C		1090	µA
	1/8 array, 45˚C		575	µA
	1/16 array, 85˚C		1020	µA
	1/16 array, 45˚C		550	µA

Notes:
1. All voltages referenced to V_{SS}.
2. Tests for I_{DD} characteristics may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to $V_{DDQ/2}$ (or to the crossing point for CK/CK#). The output timing reference voltage level is $V_{DDQ/2}$.
4. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time with the outputs open.
5. I_{DD} specifications are tested after the device is properly initialized and values are averaged at the defined cycle rate.
6. MIN (^{t}RC or ^{t}RFC) for I_{DD} measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RASmax for I_{DD} measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.
7. Measurement is taken 500ms after entering into this operating mode to provide settling time for the tester.
8. V_{DD} must not vary more than 4% if CKE is not active while any bank is active.
9. I_{DD2N} specifies DQ, DQS, and DM to be driven to a valid high or low logic level.
10. CKE must be active (HIGH) during the entire time a REFRESH command is executed. From the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge until ^{t}RFC later.
11. This limit is a nominal value and does not result in a fail. CKE is HIGH during REFRESH command period (^{t}RFC (MIN)) else CKE is LOW (for example, during standby).
12. Values for I_{DD6} 85˚C are guaranteed for the entire temperature range. All other I_{DD6} values are estimated.
13. Typical values at 25˚C, not a maximum value.
14. Self refresh is not supported for AT (85˚C to 105˚C) operation.

Figure 14: Typical Self Refresh Current vs. Temperature



Electrical Specifications – AC Operating Conditions

Table 12: Electrical Characteristics and Recommended AC Operating Conditions

Notes 1–9 apply to all the parameters in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter		Symbol	-48		-5		Unit	Notes
			Min	Max	Min	Max		
Access window of DQ from CK/CK#	CL = 3	^{t}AC	2.0	5.0	2.0	5.0	ns	
	CL = 2		2.0	6.5	2.0	6.5		
Clock cycle time	CL = 3	^{t}CK	4.8	–	5.0	–	ns	10
	CL = 2		12	–	12	–		
CK high-level width		^{t}CH	0.45	0.55	0.45	0.55	^{t}CK	
CK low-level width		^{t}CL	0.45	0.55	0.45	0.55	^{t}CK	
CKE minimum pulse width (high and low)		^{t}CKE	1	–	1	–	^{t}CK	11
Auto precharge write recovery + precharge time		^{t}DAL	–	–	–	–	–	12
DQ and DM input hold time relative to DQS (fast slew rate)		^{t}DH$_f$	0.48	–	0.48	–	ns	13, 14, 15
DQ and DM input hold time relative to DQS (slow slew rate)		^{t}DH$_s$	0.58	–	0.58	–	ns	
DQ and DM input setup time relative to DQS (fast slew rate)		^{t}DS$_f$	0.48	–	0.48	–	ns	13, 14, 15
DQ and DM input setup time relative to DQS (slow slew rate)		^{t}DS$_s$	0.58	–	0.58	–	ns	
DQ and DM input pulse width (for each input)		^{t}DIPW	1.8	–	1.8	–	ns	16
Access window of DQS from CK/CK#	CL = 3	^{t}DQSCK	2.0	5.0	2.0	5.0	ns	
	CL = 2		2.0	6.5	2.0	6.5	ns	
DQS input high pulse width		^{t}DQSH	0.4	0.6	0.4	0.6	^{t}CK	
DQS input low pulse width		^{t}DQSL	0.4	0.6	0.4	0.6	^{t}CK	
DQS–DQ skew, DQS to last DQ valid, per group, per access		^{t}DQSQ	–	0.4	–	0.4	ns	13, 17
WRITE command to first DQS latching transition		^{t}DQSS	0.75	1.25	0.75	1.25	^{t}CK	
DQS falling edge from CK rising – hold time		^{t}DSH	0.2	–	0.2	–	^{t}CK	
DQS falling edge to CK rising – setup time		^{t}DSS	0.2	–	0.2	–	^{t}CK	
Data valid output window (DVW)		n/a	^{t}QH - ^{t}DQSQ				ns	17
Half-clock period		^{t}HP	^{t}CH, ^{t}CL	–	^{t}CH, ^{t}CL	–	ns	18
Data-out High-Z window from CK/CK#	CL = 3	^{t}HZ	–	5.0	–	5.0	ns	19, 20
	CL = 2		–	6.5	–	6.5	ns	
Data-out Low-Z window from CK/CK#		^{t}LZ	1.0	–	1.0	–	ns	19

Table 12: Electrical Characteristics and Recommended AC Operating Conditions (Continued)

Notes 1–9 apply to all the parameters in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

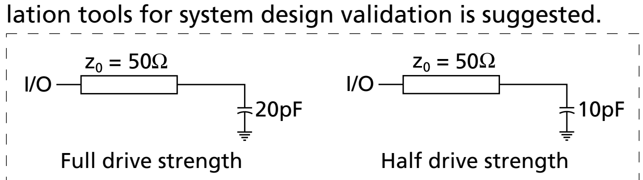
Parameter		Symbol	-48 Min	-48 Max	-5 Min	-5 Max	Unit	Notes
Address and control input hold time (fast slew rate)		^tIH_F	0.9	–	0.9	–	ns	15, 21
Address and control input hold time (slow slew rate)		^tIH_S	1.1	–	1.1	–	ns	
Address and control input setup time (fast slew rate)		^tIS_F	0.9	–	0.9	–	ns	15, 21
Address and control input setup time (slow slew rate)		^tIS_S	1.1	–	1.1	–	ns	
Address and control input pulse width		^{t}IPW	2.3	–	2.3	–	ns	16
LOAD MODE REGISTER command cycle time		^{t}MRD	2	–	2	–	^{t}CK	
DQ–DQS hold, DQS to first DQ to go nonvalid, per access		^{t}QH	^{t}HP - ^{t}QHS	–	^{t}HP - ^{t}QHS	–	ns	13, 17
Data hold skew factor		^{t}QHS	–	0.5	–	0.5	ns	
ACTIVE-to-PRECHARGE command		^{t}RAS	38.4	70,000	40	70,000	ns	22
ACTIVE to ACTIVE/ACTIVE to AUTO REFRESH command period		^{t}RC	52.8	–	55	–	ns	23
Active to read or write delay		^{t}RCD	14.4	–	15	–	ns	
Refresh period		^{t}REF	–	64	–	64	ms	29
Average periodic refresh interval: 64Mb, 128Mb, and 256Mb (x32)		^{t}REFI	–	15.6	–	15.6	µs	29
Average periodic refresh interval: 256Mb, 512Mb, 1Gb, 2Gb		^{t}REFI	–	7.8	–	7.8	µs	29
AUTO REFRESH command period		^{t}RFC	72	–	72	–	ns	
PRECHARGE command period		^{t}RP	14.4	–	15	–	ns	
DQS read preamble	CL = 3	^{t}RPRE	0.9	1.1	0.9	1.1	^{t}CK	
	CL = 2	^{t}RPRE	0.5	1.1	0.5	1.1	^{t}CK	
DQS read postamble		^{t}RPST	0.4	0.6	0.4	0.6	^{t}CK	
Active bank *a* to active bank *b* command		^{t}RRD	9.6	–	10	–	ns	
Read of SRR to next valid command		^{t}SRC	CL + 1	–	CL + 1	–	^{t}CK	
SRR to read		^{t}SRR	2	–	2	–	^{t}CK	
Internal temperature sensor valid temperature output enable		^{t}TQ	2	–	2	–	ms	
DQS write preamble		^{t}WPRE	0.25	–	0.25	–	^{t}CK	
DQS write preamble setup time		^{t}WPRES	0	–	0	–	ns	24, 25
DQS write postamble		^{t}WPST	0.4	0.6	0.4	0.6	^{t}CK	26
Write recovery time		^{t}WR	14.4	–	15	–	ns	27

Table 12: Electrical Characteristics and Recommended AC Operating Conditions (Continued)

Notes 1–9 apply to all the parameters in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter	Symbol	-48		-5		Unit	Notes
		Min	Max	Min	Max		
Internal WRITE-to-READ command delay	^{t}WTR	2	–	2	–	^{t}CK	
Exit power-down mode to first valid command	^{t}XP	2	–	2	–	^{t}CK	
Exit self refresh to first valid command	^{t}XSR	110	–	112.5	–	ns	28

Notes:
1. All voltages referenced to V_{SS}.
2. All parameters assume proper device initialization.
3. Tests for AC timing and electrical AC and DC characteristics may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage ranges specified.
4. The circuit shown below represents the timing reference load used in defining the relevant timing parameters of the device. It is not intended to be either a precise representation of the typical system environment or a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to system environment. Specifications are correlated to production test conditions (generally a coaxial transmission line terminated at the tester electronics). For the half-strength driver with a nominal 10pF load, parameters ^{t}AC and ^{t}QH are expected to be in the same range. However, these parameters are not subject to production test but are estimated by design/characterization. Use of IBIS or other simulation tools for system design validation is suggested.



5. The CK/CK# input reference voltage level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference voltage level for signals other than CK/CK# is $V_{DDQ/2}$.
6. A CK and CK# input slew rate ≥1 V/ns (2 V/ns if measured differentially) is assumed for all parameters.
7. All AC timings assume an input slew rate of 1 V/ns.
8. CAS latency definition: with CL = 2, the first data element is valid at (^{t}CK + ^{t}AC) after the clock at which the READ command was registered; for CL = 3, the first data element is valid at (2 × ^{t}CK + ^{t}AC) after the first clock at which the READ command was registered.
9. Timing tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to $V_{DDQ/2}$ or to the crossing point for CK/CK#. The output timing reference voltage level is $V_{DDQ/2}$.
10. Clock frequency change is only permitted during clock stop, power-down, or self refresh mode.
11. In cases where the device is in self refresh mode for ^{t}CKE, ^{t}CKE starts at the rising edge of the clock and ends when CKE transitions HIGH.
12. ^{t}DAL = (^{t}WR/^{t}CK) + (^{t}RP/^{t}CK): for each term, if not already an integer, round up to the next highest integer.

13. Referenced to each output group: for x16, LDQS with DQ[7:0]; and UDQS with DQ[15:8]. For x32, DQS0 with DQ[7:0]; DQS1 with DQ[15:8]; DQS2 with DQ[23:16]; and DQS3 with DQ[31:24].
14. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/DM/DQS slew rate is less than 1.0 V/ns, timing must be derated: 50ps must be added to ^tDS and ^tDH for each 100 mV/ns reduction in slew rate. If the slew rate exceeds 4 V/ns, functionality is uncertain.
15. The transition time for input signals (CAS#, CKE, CS#, DM, DQ, DQS, RAS#, WE#, and addresses) are measured between $V_{IL(DC)}$ to $V_{IH(AC)}$ for rising input signals and $V_{IH(DC)}$ to $V_{IL(AC)}$ for falling input signals.
16. These parameters guarantee device timing but are not tested on each device.
17. The valid data window is derived by achieving other specifications: ^tHP ($^tCK/2$), ^tDQSQ, and ^tQH (^tHP - ^tQHS). The data valid window derates directly proportional with the clock duty cycle and a practical data valid window can be derived. The clock is provided a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio.
18. ^tHP (MIN) is the lesser of ^tCL (MIN) and ^tCH (MIN) actually applied to the device CK and CK# inputs, collectively.
19. ^tHZ and ^tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (^tHZ) or begins driving (^tLZ).
20. ^tHZ (MAX) will prevail over ^tDQSCK (MAX) + ^tRPST (MAX) condition.
21. Fast command/address input slew rate ≥1 V/ns. Slow command/address input slew rate ≥0.5 V/ns. If the slew rate is less than 0.5 V/ns, timing must be derated: ^tIS has an additional 50ps per each 100 mV/ns reduction in slew rate from the 0.5 V/ns. ^tIH has 0ps added, therefore, it remains constant. If the slew rate exceeds 4.5 V/ns, functionality is uncertain.
22. READs and WRITEs with auto precharge must not be issued until ^tRAS (MIN) can be satisfied prior to the internal PRECHARGE command being issued.
23. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime.
24. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
25. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic low) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^tDQSS.
26. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
27. At least 1 clock cycle is required during ^tWR time when in auto precharge mode.
28. Clock must be toggled a minimum of two times during the ^tXSR period.
29. For the Automotive Temperature parts, ^tREF = ^tREF /2 and ^tREF I = ^tREF I/2 .

Output Drive Characteristics

Table 13: Target Output Drive Characteristics (Full Strength)

Notes 1–2 apply to all values; characteristics are specified under best and worst process variations/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	2.80	18.53	–2.80	–18.53
0.20	5.60	26.80	–5.60	–26.80
0.30	8.40	32.80	–8.40	–32.80
0.40	11.20	37.05	–11.20	–37.05
0.50	14.00	40.00	–14.00	–40.00
0.60	16.80	42.50	–16.80	–42.50
0.70	19.60	44.57	–19.60	–44.57
0.80	22.40	46.50	–22.40	–46.50
0.85	23.80	47.48	–23.80	–47.48
0.90	23.80	48.50	–23.80	–48.50
0.95	23.80	49.40	–23.80	–49.40
1.00	23.80	50.05	–23.80	–50.05
1.10	23.80	51.35	–23.80	–51.35
1.20	23.80	52.65	–23.80	–52.65
1.30	23.80	53.95	–23.80	–53.95
1.40	23.80	55.25	–23.80	–55.25
1.50	23.80	56.55	–23.80	–56.55
1.60	23.80	57.85	–23.80	–57.85
1.70	23.80	59.15	–23.80	–59.15
1.80	–	60.45	–	–60.45
1.90	–	61.75	–	–61.75

Notes:
1. Based on nominal impedance of 25Ω (full strength) at $V_{DDQ}/2$.
2. The full variation in driver current from minimum to maximum, due to process, voltage, and temperature, will lie within the outer bounding lines of the I-V curves.

Table 14: Target Output Drive Characteristics (Three-Quarter Strength)

Notes 1–3 apply to all values; characteristics are specified under best and worst process variations/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	1.96	12.97	–1.96	–12.97
0.20	3.92	18.76	–3.92	–18.76
0.30	5.88	22.96	–5.88	–22.96
0.40	7.84	25.94	–7.84	–25.94
0.50	9.80	28.00	–9.80	–28.00
0.60	11.76	29.75	–11.76	–29.75
0.70	13.72	31.20	–13.72	–31.20
0.80	15.68	32.55	–15.68	–32.55
0.85	16.66	33.24	–16.66	–33.24
0.90	16.66	33.95	–16.66	–33.95
0.95	16.66	34.58	–16.66	–34.58
1.00	16.66	35.04	–16.66	–35.04
1.10	16.66	35.95	–16.66	–35.95
1.20	16.66	36.86	–16.66	–36.86
1.30	16.66	37.77	–16.66	–37.77
1.40	16.66	38.68	–16.66	–38.68
1.50	16.66	39.59	–16.66	–39.59
1.60	16.66	40.50	–16.66	–40.50
1.70	16.66	41.41	–16.66	–41.41
1.80	–	42.32	–	–42.32
1.90	–	43.23	–	–43.23

Notes:
1. Based on nominal impedance of 37Ω (three-quarter drive strength) at $V_{DDQ}/2$.
2. The full variation in driver current from minimum to maximum, due to process, voltage, and temperature, will lie within the outer bounding lines of the I-V curves.
3. Contact factory for availability of three-quarter drive strength.

Table 15: Target Output Drive Characteristics (One-Half Strength)

Notes 1–3 apply to all values; characteristics are specified under best and worst process variations/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	1.27	8.42	–1.27	–8.42
0.20	2.55	12.30	–2.55	–12.30
0.30	3.82	14.95	–3.82	–14.95
0.40	5.09	16.84	–5.09	–16.84
0.50	6.36	18.20	–6.36	–18.20
0.60	7.64	19.30	–7.64	–19.30
0.70	8.91	20.30	–8.91	–20.30
0.80	10.16	21.20	–10.16	–21.20
0.85	10.80	21.60	–10.80	–21.60
0.90	10.80	22.00	–10.80	–22.00
0.95	10.80	22.45	–10.80	–22.45
1.00	10.80	22.73	–10.80	–22.73
1.10	10.80	23.21	–10.80	–23.21
1.20	10.80	23.67	–10.80	–23.67
1.30	10.80	24.14	–10.80	–24.14
1.40	10.80	24.61	–10.80	–24.61
1.50	10.80	25.08	–10.80	–25.08
1.60	10.80	25.54	–10.80	–25.54
1.70	10.80	26.01	–10.80	–26.01
1.80	–	26.48	–	–26.48
1.90	–	26.95	–	–26.95

Notes:
1. Based on nominal impedance of 55Ω (one-half drive strength) at $V_{DDQ}/2$.
2. The full variation in driver current from minimum to maximum, due to process, voltage, and temperature, will lie within the outer bounding lines of the I-V curves.
3. The I-V curve for one-quarter drive strength is approximately 50% of one-half drive strength.

Functional Description

The Mobile LPDDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O. Single read or write access for the device consists of a single 2*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 device has two data strobes, one for the lower byte and one for the upper byte; the x32 device has four data strobes, one per byte.

The LPDDR device operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the device are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The device provides for programmable READ or WRITE burst lengths of 2, 4, 8, or 16. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of LPDDR supports concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. Deep power-down mode is offered to achieve maximum power reduction by eliminating the power of the memory array. Data will not be retained after the device enters deep power-down mode.

Two self refresh features, temperature-compensated self refresh (TCSR) and partial-array self refresh (PASR), offer additional power savings. TCSR is controlled by the automatic on-chip temperature sensor. PASR can be customized using the extended mode register settings. The two features can be combined to achieve even greater power savings.

The DLL that is typically used on standard DDR devices is not necessary on LPDDR devices. It has been omitted to save power.

Commands

A quick reference for available commands is provided in Table 16 and Table 17 (page 41), followed by a written description of each command. Three additional truth tables (Table 18 (page 47), Table 19 (page 49), and Table 20 (page 51)) provide CKE commands and current/next state information.

Table 16: Truth Table – Commands

CKE is HIGH for all commands shown except SELF REFRESH and DEEP POWER-DOWN; all states and sequences not shown are reserved and/or illegal

Name (Function)	CS#	RAS#	CAS#	WE#	Address	Notes
DESELECT (NOP)	H	X	X	X	X	1
NO OPERATION (NOP)	L	H	H	H	X	1
ACTIVE (select bank and activate row)	L	L	H	H	Bank/row	2
READ (select bank and column, and start READ burst)	L	H	L	H	Bank/column	3
WRITE (select bank and column, and start WRITE burst)	L	H	L	L	Bank/column	3
BURST TERMINATE or DEEP POWER-DOWN (enter deep power-down mode)	L	H	H	L	X	4, 5
PRECHARGE (deactivate row in bank or banks)	L	L	H	L	Code	6
AUTO REFRESH (refresh all or single bank) or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	7, 8
LOAD MODE REGISTER	L	L	L	L	Op-code	9

Notes:
1. DESELECT and NOP are functionally interchangeable.
2. BA0–BA1 provide bank address and A[0:*I*] provide row address (where *I* = the most significant address bit for each configuration).
3. BA0–BA1 provide bank address; A[0:*I*] provide column address (where *I* = the most significant address bit for each configuration); A10 HIGH enables the auto precharge feature (nonpersistent); A10 LOW disables the auto precharge feature.
4. Applies only to READ bursts with auto precharge disabled; this command is undefined and should not be used for READ bursts with auto precharge enabled and for WRITE bursts.
5. This command is a BURST TERMINATE if CKE is HIGH and DEEP POWER-DOWN if CKE is LOW.
6. A10 LOW: BA0–BA1 determine which bank is precharged.
   A10 HIGH: all banks are precharged and BA0–BA1 are "Don't Care."
7. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
8. Internal refresh counter controls row addressing; in self refresh mode all inputs and I/Os are "Don't Care" except for CKE.
9. BA0–BA1 select the standard mode register, extended mode register, or status register.

Table 17: DM Operation Truth Table

Name (Function)	DM	DQ	Notes
Write enable	L	Valid	1, 2
Write inhibit	H	X	1, 2

Notes:
1. Used to mask write data; provided coincident with the corresponding data.
2. All states and sequences not shown are reserved and/or illegal.

DESELECT

The DESELECT function (CS# HIGH) prevents new commands from being executed by the device. Operations already in progress are not affected.

NO OPERATION

The NO OPERATION (NOP) command is used to instruct the selected device to perform a NOP. This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

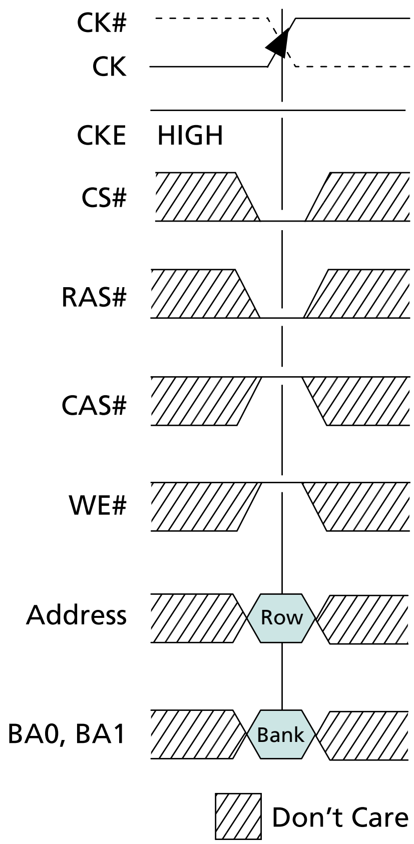
LOAD MODE REGISTER

The mode registers are loaded via inputs A[0:*n*]. See mode register descriptions in Standard Mode Register and Extended Mode Register. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to activate a row in a particular bank for a subsequent access. The values on the BA0 and BA1 inputs select the bank, and the address provided on inputs A[0:*n*] selects the row. This row remains active for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

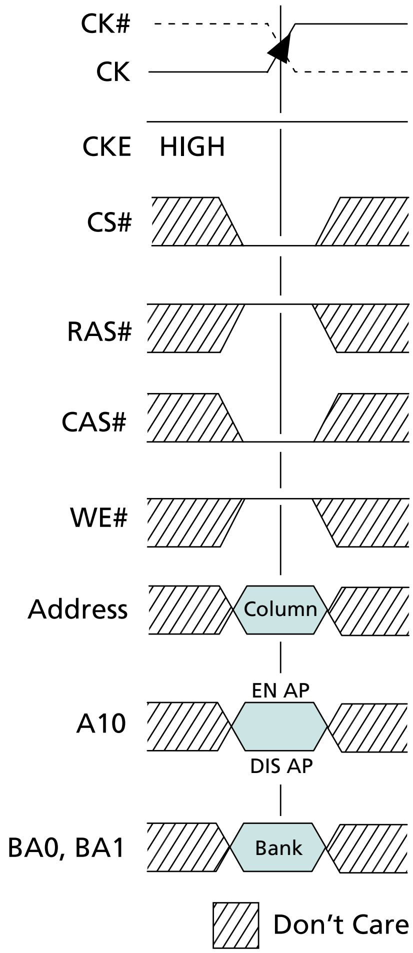
Figure 15: ACTIVE Command



READ

The READ command is used to initiate a burst read access to an active row. The values on the BA0 and BA1 inputs select the bank; the address provided on inputs A[I:0] (where I = the most significant column address bit for each configuration) selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

Figure 16: READ Command



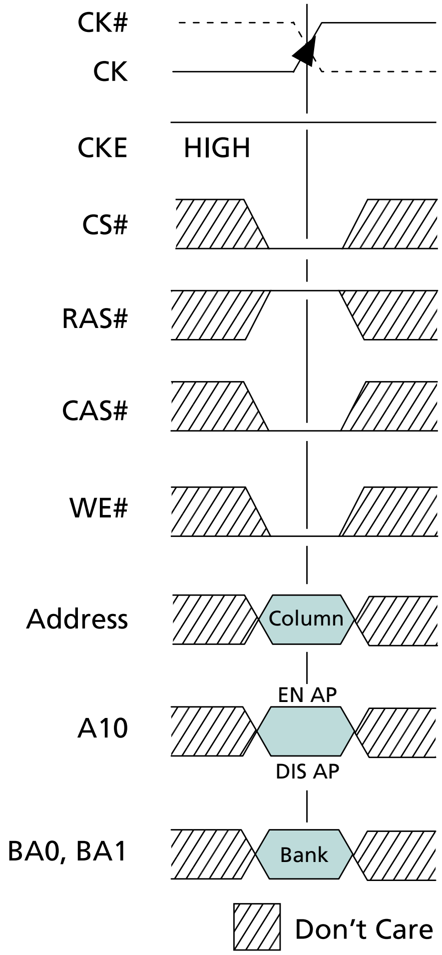
Note: 1. EN AP = enable auto precharge; DIS AP = disable auto precharge.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The values on the BA0 and BA1 inputs select the bank; the address provided on inputs A[*I*:0] (where *I* = the most significant column address bit for each configuration) selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQ is written to the memory array, subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

If a WRITE or a READ is in progress, the entire data burst must be complete prior to stopping the clock (see Clock Change Frequency (page 100)). A burst completion for WRITEs is defined when the write postamble and ^{t}WR or ^{t}WTR are satisfied.

Figure 17: WRITE Command

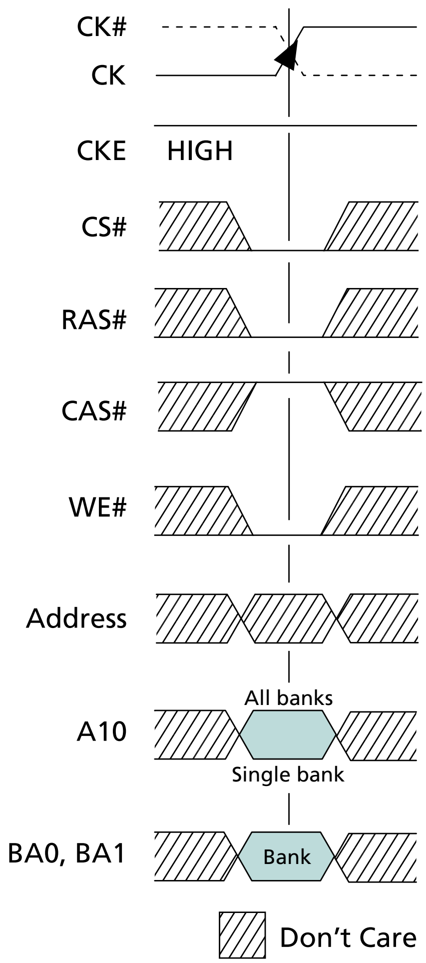


Note: 1. EN AP = enable auto precharge; DIS AP = disable auto precharge.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks will be precharged, and in the case where only one bank is precharged, inputs BA0 and BA1 select the bank. Otherwise, BA0 and BA1 are treated as “Don’t Care.” After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Figure 18: PRECHARGE Command



Note: 1. If A10 is HIGH, bank address becomes "Don't Care."

BURST TERMINATE

The BURST TERMINATE command is used to truncate READ bursts with auto precharge disabled. The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as described in READ Operation. The open page from which the READ was terminated remains open.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the device and is analogous to CAS#-BEFORE-RAS# (CBR) REFRESH in FPM/EDO DRAM. The AUTO REFRESH command is nonpersistent and must be issued each time a refresh is required.

Addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an AUTO REFRESH command.

For improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. The auto refresh period begins when the AUTO REFRESH command is registered and ends ^{t}RFC later.

SELF REFRESH

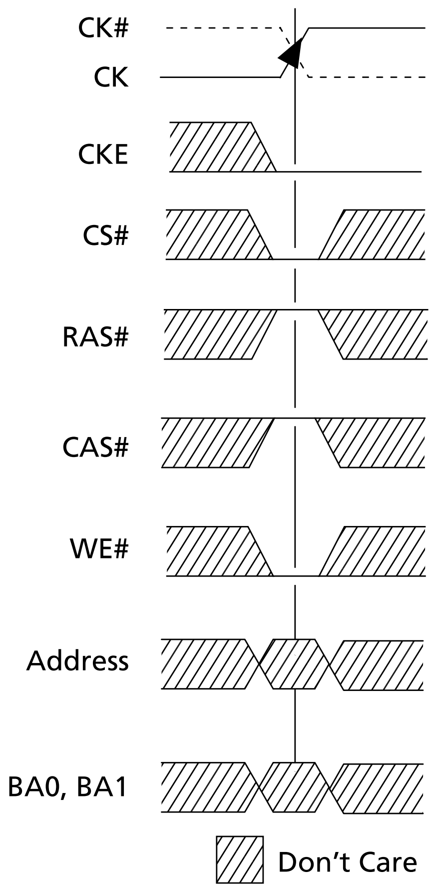
The SELF REFRESH command is used to place the device in self refresh mode; self refresh mode is used to retain data in the memory device while the rest of the system is powered down. When in self refresh mode, the device retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command, except that CKE is disabled (LOW). After the SELF REFRESH command is registered, all inputs to the device become “Don’t Care” with the exception of CKE, which must remain LOW.

Micron recommends that, prior to self refresh entry and immediately upon self refresh exit, the user perform a burst auto refresh cycle for the number of refresh rows. Alternatively, if a distributed refresh pattern is used, this pattern should be immediately resumed upon self refresh exit.

DEEP POWER-DOWN

The DEEP POWER-DOWN (DPD) command is used to enter DPD mode, which achieves maximum power reduction by eliminating the power to the memory array. Data will not be retained when the device enters DPD mode. The DPD command is the same as a BURST TERMINATE command with CKE LOW.

Figure 19: DEEP POWER-DOWN Command



Truth Tables

Table 18: Truth Table – Current State Bank *n* – Command to Bank *n*

Notes 1–6 apply to all parameters in this table

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
Row active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (auto pre-charge disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10, 12
	L	L	H	L	PRECHARGE (truncate READ burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9
Write (auto pre-charge disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start PRECHARGE)	8, 11

Notes:
1. This table applies when CKE_{n-1} was HIGH, CKE_n is HIGH and after ^tXSR has been met (if the previous state was self refresh), after ^tXP has been met (if the previous state was power-down), or after a full initialization (if the previous state was deep power-down).
2. This table is bank-specific, except where noted (for example, the current state is for a specific bank and the commands shown are supported for that bank when in that state). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and ^tRP has been met.

   Row active: A row in the bank has been activated, and ^tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated with auto precharge disabled and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated with auto precharge disabled and has not yet terminated or been terminated.
4. The states listed below must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or supported commands to the other bank, must be issued on any clock edge occurring during these states. Supported commands to any other bank are determined by that bank's current state.

   Precharging: Starts with registration of a PRECHARGE command and ends when ^tRP is met. After ^tRP is met, the bank will be in the idle state.

   Row activating: Starts with registration of an ACTIVE command and ends when ^tRCD is met. After ^tRCD is met, the bank will be in the row active state.

Read with auto-precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when ^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.

Write with auto-precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when ^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.

5. The states listed below must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an AUTO REFRESH command and ends when ^{t}RFC is met. After ^{t}RFC is met, the device will be in the all banks idle state.

   Accessing mode register: Starts with registration of a LOAD MODE REGISTER command and ends when ^{t}MRD has been met. After ^{t}MRD is met, the device will be in the all banks idle state.

   Precharging all: Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. After ^{t}RP is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle, and bursts are not in progress.
8. May or may not be bank-specific; if multiple banks need to be precharged, each must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
10. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Requires appropriate DM masking.
12. A WRITE command can be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

Table 19: Truth Table – Current State Bank *n* – Command to Bank *m*

Notes 1–6 apply to all parameters in this table

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any command supported to bank *m*	
Row activating, active, or pre-charging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	
	L	H	L	L	WRITE (select column and start WRITE burst)	
	L	L	H	L	PRECHARGE	
Read (auto pre-charge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Write (auto pre-charge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	
	L	H	L	L	WRITE (select column and start new WRITE burst)	
	L	L	H	L	PRECHARGE	
Read (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Write (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	
	L	H	L	L	WRITE (select column and start new WRITE burst)	
	L	L	H	L	PRECHARGE	

Notes:

1. This table applies when CKE_{n-1} was HIGH, CKE_n is HIGH and after ^tXSR has been met (if the previous state was self refresh), after ^tXP has been met (if the previous state was power-down) or after a full initialization (if the previous state was deep power-down).
2. This table describes alternate bank operation, except where noted (for example, the current state is for bank *n* and the commands shown are those supported for issue to bank *m*, assuming that bank *m* is in such a state that the given command is supported). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and ^tRP has been met.

   Row active: A row in the bank has been activated, and ^tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated and has not yet terminated or been terminated.

   3a. Both the read with auto precharge enabled state or the write with auto precharge enabled state can be broken into two parts: the access period and the precharge period.

For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when ${}^{t}WR$ ends, with ${}^{t}WR$ measured as if auto precharge was disabled. The access period starts with registration of the command and ends when the precharge period (or ${}^{t}RP$) begins. This device supports concurrent auto precharge such that when a read with auto precharge is enabled or a write with auto precharge is enabled, any command to other banks is supported, as long as that command does not interrupt the read or write data transfer already in process. In either case, all other related limitations apply (i.e., contention between read data and write data must be avoided).

3b. The minimum delay from a READ or WRITE command (with auto precharge enabled) to a command to a different bank is summarized below.

From Command	To Command	Minimum Delay (with Concurrent Auto Precharge)
WRITE with Auto Precharge	READ or READ with auto precharge WRITE or WRITE with auto precharge PRECHARGE ACTIVE	[1 + (BL/2)] ${}^{t}CK$ + ${}^{t}WTR$ (BL/2) ${}^{t}CK$ 1 ${}^{t}CK$ 1 ${}^{t}CK$
READ with Auto Precharge	READ or READ with auto precharge WRITE or WRITE with auto precharge PRECHARGE ACTIVE	(BL/2) × ${}^{t}CK$ [CL + (BL/2)] ${}^{t}CK$ 1 ${}^{t}CK$ 1 ${}^{t}CK$

4. AUTO REFRESH and LOAD MODE REGISTER commands can only be issued when all banks are idle.
5. All states and sequences not shown are illegal or reserved.
6. Requires appropriate DM masking.
7. A WRITE command can be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

Table 20: Truth Table – CKE

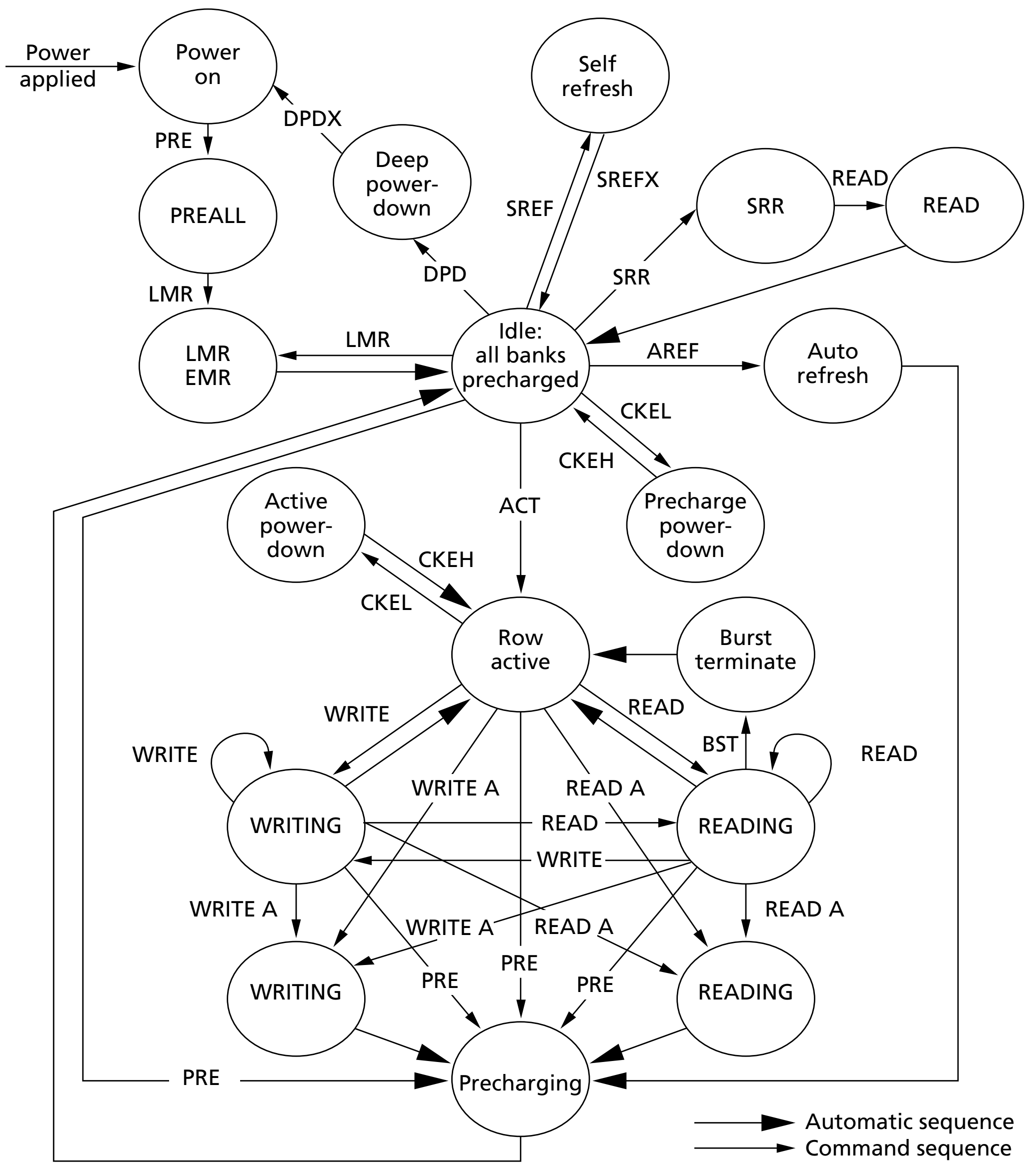
Notes 1–4 apply to all parameters in this table

Current State	CKE_{n-1}	CKE_n	$COMMAND_n$	$ACTION_n$	Notes
Active power-down	L	L	X	Maintain active power-down	
Deep power-down	L	L	X	Maintain deep power-down	
Precharge power-down	L	L	X	Maintain precharge power-down	
Self refresh	L	L	X	Maintain self refresh	
Active power-down	L	H	DESELECT or NOP	Exit active power-down	5
Deep power-down	L	H	DESELECT or NOP	Exit deep power-down	6
Precharge power-down	L	H	DESELECT or NOP	Exit precharge power-down	
Self refresh	L	H	DESELECT or NOP	Exit self refresh	5, 7
Bank(s) active	H	L	DESELECT or NOP	Active power-down entry	
All banks idle	H	L	BURST TERMINATE	Deep power-down entry	
All banks idle	H	L	DESELECT or NOP	Precharge power-down entry	
All banks idle	H	L	AUTO REFRESH	Self refresh entry	
	H	H	See Table 19 (page 49)		
	H	H	See Table 19 (page 49)		

Notes:
1. CKE_n is the logic state of CKE at clock edge *n*; CKE_{n-1} was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge *n*.
3. $COMMAND_n$ is the command registered at clock edge *n*, and $ACTION_n$ is a result of $COMMAND_n$.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT or NOP commands should be issued on each clock edge occurring during the ^tXP or ^tXSR period.
6. After exiting deep power-down mode, a full DRAM initialization sequence is required.
7. The clock must toggle at least two times during the ^tXSR period.

State Diagram

Figure 20: Simplified State Diagram



ACT = ACTIVE
AREF = AUTO REFRESH
BST = BURST TERMINATE
CKEH = Exit power-down
CKEL = Enter power-down
DPD = Enter deep power-down

DPDX = Exit deep power-down
EMR = LOAD EXTENDED MODE REGISTER
LMR = LOAD MODE REGISTER
PRE = PRECHARGE
PREALL = PRECHARGE all banks
READ = READ w/o auto precharge

READ A = READ w/ auto precharge
SREF = Enter self refresh
SREFX = Exit self refresh
SRR = STATUS REGISTER READ
WRITE = WRITE w/o auto precharge
WRITE A = WRITE w/ auto precharge

Initialization

Prior to normal operation, the device must be powered up and initialized in a predefined manner. Using initialization procedures other than those specified will result in undefined operation.

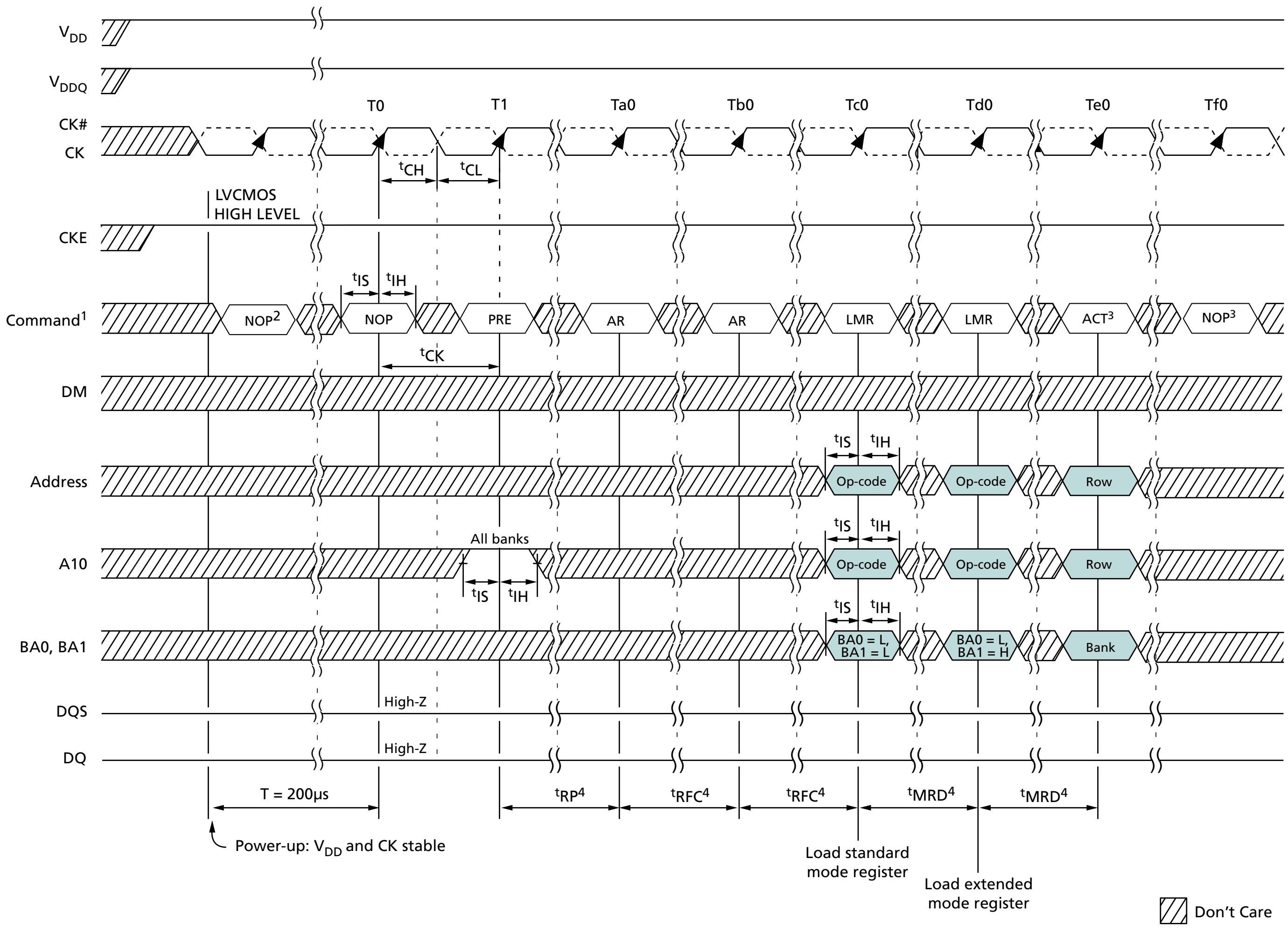
If there is an interruption to the device power, the device must be re-initialized using the initialization sequence described below to ensure proper functionality of the device.

To properly initialize the device, this sequence must be followed:

1. The core power (V_{DD}) and I/O power (V_{DDQ}) must be brought up simultaneously. It is recommended that V_{DD} and V_{DDQ} be from the same power source, or V_{DDQ} must never exceed V_{DD}. Standard initialization requires that CKE be asserted HIGH (see Figure 21 (page 54)). Alternatively, initialization can be completed with CKE LOW provided that CKE transitions HIGH ^tIS prior to T0 (see Figure 22 (page 55)).
2. When power supply voltages are stable and the CKE has been driven HIGH, it is safe to apply the clock.
3. When the clock is stable, a 200µs minimum delay is required by the Mobile LPDDR prior to applying an executable command. During this time, NOP or DESELECT commands must be issued on the command bus.
4. Issue a PRECHARGE ALL command.
5. Issue NOP or DESELECT commands for at least ^tRP time.
6. Issue an AUTO REFRESH command followed by NOP or DESELECT commands for at least ^tRFC time. Issue a second AUTO REFRESH command followed by NOP or DESELECT commands for at least ^tRFC time. Two AUTO REFRESH commands must be issued. Typically, both of these commands are issued at this stage as described above.
7. Using the LOAD MODE REGISTER command, load the standard mode register as desired.
8. Issue NOP or DESELECT commands for at least ^tMRD time.
9. Using the LOAD MODE REGISTER command, load the extended mode register to the desired operating modes. Note that the sequence in which the standard and extended mode registers are programmed is not critical.
10. Issue NOP or DESELECT commands for at least ^tMRD time.

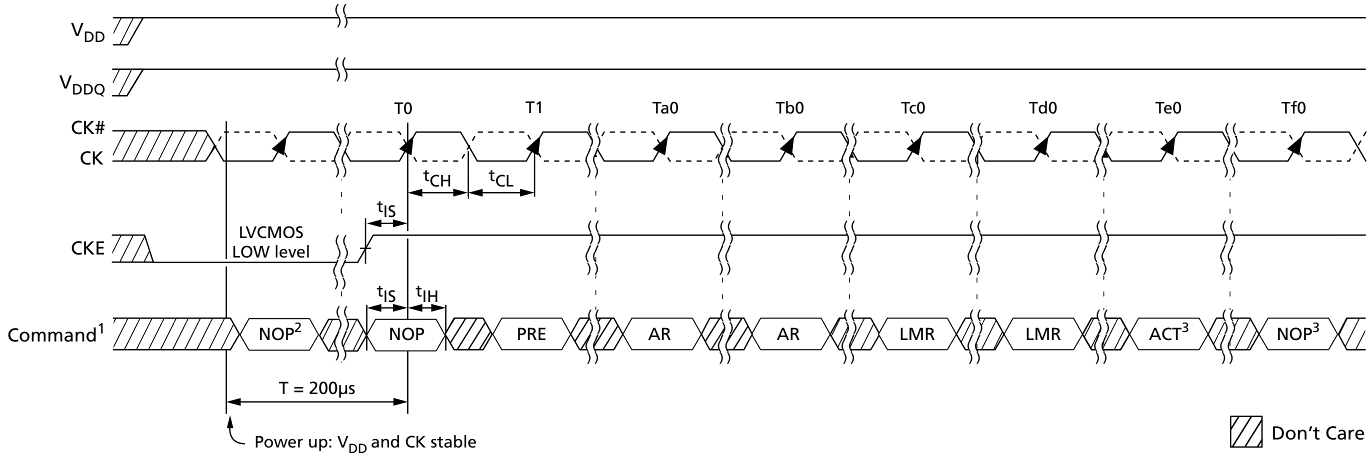
After steps 1–10 are completed, the device has been properly initialized and is ready to receive any valid command.

Figure 21: Initialize and Load Mode Registers



Notes:
1. PRE = PRECHARGE command; LMR = LOAD MODE REGISTER command; AR = AUTO REFRESH command; ACT = ACTIVE command.
2. NOP or DESELECT commands are required for at least 200µs.
3. Other valid commands are possible.
4. NOPs or DESELECTs are required during this time.

Figure 22: Alternate Initialization with CKE LOW



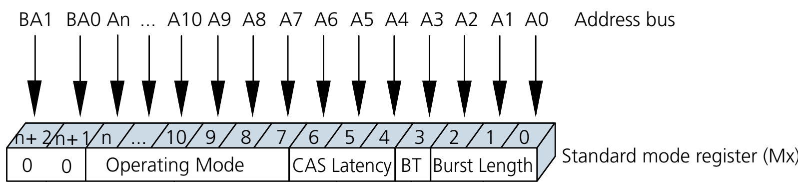
Notes:
1. PRE = PRECHARGE command; LMR = LOAD MODE REGISTER command; AR = AUTO REFRESH command; ACT = ACTIVE command.
2. NOP or DESELECT commands are required for at least 200µs.
3. Other valid commands are possible.

Standard Mode Register

The standard mode register bit definition enables the selection of burst length, burst type, CAS latency (CL), and operating mode, as shown in Figure 23. Reserved states should not be used as this may result in setting the device into an unknown state or cause incompatibility with future versions of LPDDR devices. The standard mode register is programmed via the LOAD MODE REGISTER command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again, until the device goes into deep power-down mode, or until the device loses power.

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait ^{t}MRD before initiating the subsequent operation. Violating any of these requirements will result in unspecified operation.

Figure 23: Standard Mode Register Definition



Mn + 2	Mn + 1	Mode Register Definition
0	0	Standard mode register
0	1	Status register
1	0	Extended mode register
1	1	Reserved

M2	M1	M0	Burst Length M3 = 0	Burst Length M3 = 1
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	16	16
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

Mn	...	M10	M9	M8	M7	Operating Mode
0		0	0	0	0	Normal operation
–		–	–	–	–	All other states reserved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

Note: 1. The integer *n* is equal to the most significant address bit.

Burst Length

Read and write accesses to the device are burst-oriented, and the burst length (BL) is programmable. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, 8, or 16 locations are available for both sequential and interleaved burst types.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap when a boundary is reached. The block is uniquely selected by A[*i*:1] when BL = 2, by A[*i*:2] when BL = 4, by A[*i*:3] when BL = 8, and by A[*i*:4] when BL = 16, where A*i* is the most significant column address bit for a given configuration. The remaining (least significant) address bits are used to specify the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst can be programmed to be either sequential or interleaved via the standard mode register.

The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address.

Table 21: Burst Definition Table

Burst Length	Starting Column Address				Order of Accesses Within a Burst	
					Type = Sequential	Type = Interleaved
2				**A0**		
				0	0-1	0-1
				1	1-0	1-0
4			**A1**	**A0**		
			0	0	0-1-2-3	0-1-2-3
			0	1	1-2-3-0	1-0-3-2
			1	0	2-3-0-1	2-3-0-1
			1	1	3-0-1-2	3-2-1-0
8		**A2**	**A1**	**A0**		
		0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
		0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
		0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
		0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
		1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
		1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
		1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
		1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
16	**A3**	**A2**	**A1**	**A0**		

Table 21: Burst Definition Table (Continued)

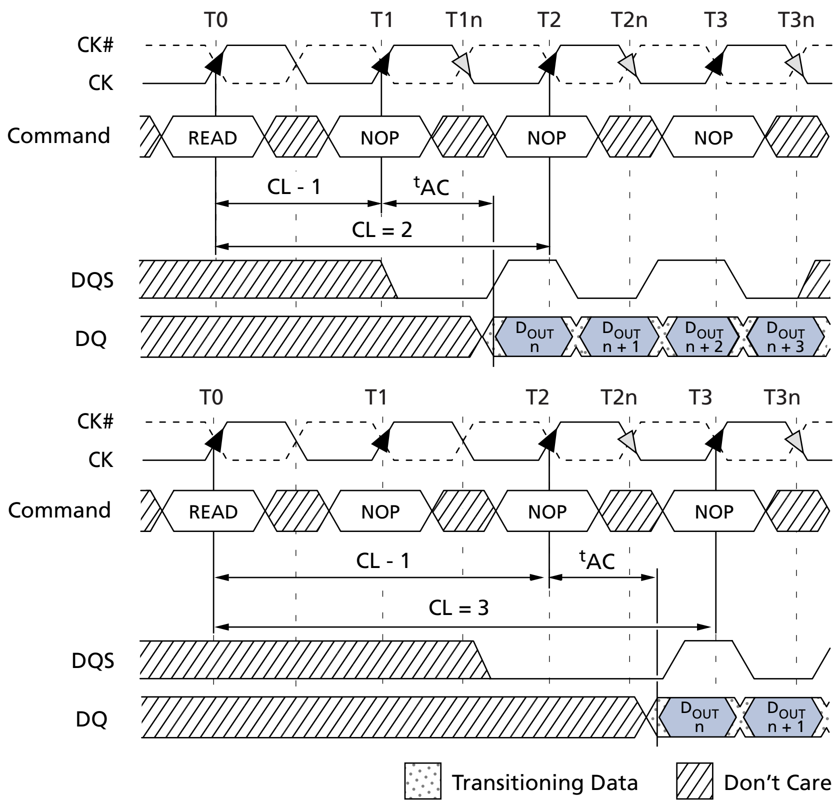
Burst Length	Starting Column Address				Order of Accesses Within a Burst	
					Type = Sequential	Type = Interleaved
	0	0	0	0	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F
	0	0	0	1	1-2-3-4-5-6-7-8-9-A-B-C-D-E-F-0	1-0-3-2-5-4-7-6-9-8-B-A-D-C-F-E
	0	0	1	0	2-3-4-5-6-7-8-9-A-B-C-D-E-F-0-1	2-3-0-1-6-7-4-5-A-B-8-9-E-F-C-D
	0	0	1	1	3-4-5-6-7-8-9-A-B-C-D-E-F-0-1-2	3-2-1-0-7-6-5-4-B-A-9-8-F-E-D-C
	0	1	0	0	4-5-6-7-8-9-A-B-C-D-E-F-0-1-2-3	4-5-6-7-0-1-2-3-C-D-E-F-8-9-A-B
	0	1	0	1	5-6-7-8-9-A-B-C-D-E-F-0-1-2-3-4	5-4-7-6-1-0-3-2-D-C-F-E-9-8-B-A
	0	1	1	0	6-7-8-9-A-B-C-D-E-F-0-1-2-3-4-5	6-7-4-5-2-3-0-1-E-F-C-D-A-B-8-9
	0	1	1	1	7-8-9-A-B-C-D-E-F-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0-F-E-D-C-B-A-9-8
	1	0	0	0	8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7	8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7
	1	0	0	1	9-A-B-C-D-E-F-0-1-2-3-4-5-6-7-8	9-8-B-A-D-C-F-E-1-0-3-2-5-4-7-6
	1	0	1	0	A-B-C-D-E-F-0-1-2-3-4-5-6-7-8-9	A-B-8-9-E-F-C-D-2-3-0-1-6-7-4-5
	1	0	1	1	B-C-D-E-F-0-1-2-3-4-5-6-7-8-9-A	B-A-9-8-F-E-D-C-3-2-1-0-7-6-5-4
	1	1	0	0	C-D-E-F-0-1-2-3-4-5-6-7-8-9-A-B	C-D-E-F-8-9-A-B-4-5-6-7-0-1-2-3
	1	1	0	1	D-E-F-0-1-2-3-4-5-6-7-8-9-A-B-C	D-C-F-E-9-8-B-A-5-4-7-6-1-0-3-2
	1	1	1	0	E-F-0-1-2-3-4-5-6-7-8-9-A-B-C-D	E-F-C-D-A-B-8-9-6-7-4-5-2-3-0-1
	1	1	1	1	F-0-1-2-3-4-5-6-7-8-9-A-B-C-D-E	F-E-D-C-B-A-9-8-7-6-5-4-3-2-1-0

CAS Latency

The CAS latency (CL) is the delay, in clock cycles, between the registration of a READ command and the availability of the first output data. The latency can be set to 2 or 3 clocks, as shown in Figure 24 (page 59).

For CL = 3, if the READ command is registered at clock edge n, then the data will be nominally available at (n + 2 clocks + ^{t}AC). For CL = 2, if the READ command is registered at clock edge n, then the data will be nominally available at (n + 1 clock + ^{t}AC).

Figure 24: CAS Latency



Operating Mode

The normal operating mode is selected by issuing a LOAD MODE REGISTER command with bits A[*n*:7] each set to zero, and bits A[6:0] set to the desired values.

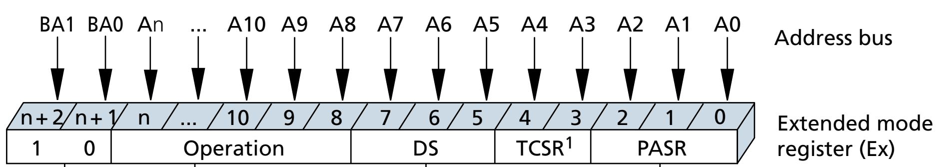
All other combinations of values for A[*n*:7] are reserved for future use. Reserved states should not be used because unknown operation or incompatibility with future versions may result.

Extended Mode Register

The EMR controls additional functions beyond those set by the mode registers. These additional functions include drive strength, TCSR, and PASR.

The EMR is programmed via the LOAD MODE REGISTER command with BA0 = 0 and BA1 = 1. Information in the EMR will be retained until it is programmed again, the device goes into deep power-down mode, or the device loses power.

Figure 25: Extended Mode Register



En + 2	En + 1	Mode Register Definition
0	0	Standard mode register
0	1	Status register
1	0	Extended mode register
1	1	Reserved

E7	E6	E5	Drive Strength
0	0	0	Full strength
0	0	1	1/2 strength
0	1	0	1/4 strength
0	1	1	3/4 strength
1	0	0	3/4 strength
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

En	...	E10	E9	E8	E7–E0	
0	0	0	0	0	Valid	Normal AR operation
–	–	–	–	–	–	All other states reserved

E2	E1	E0	Partial-Array Self Refresh Coverage
0	0	0	Full array
0	0	1	1/2 array
0	1	0	1/4 array
0	1	1	Reserved
1	0	0	Reserved
1	0	1	1/8 array
1	1	0	1/16 array
1	1	1	Reserved

Notes: 1. On-die temperature sensor is used in place of TCSR. Setting these bits will have no effect.

2. The integer *n* is equal to the most significant address bit.

Temperature-Compensated Self Refresh

This device includes a temperature sensor that is implemented for automatic control of the self refresh oscillator. Programming the temperature-compensated self refresh (TCSR) bits will have no effect on the device. The self refresh oscillator will continue to refresh at the optimal factory-programmed rate for the device temperature.

Partial-Array Self Refresh

For further power savings during self refresh, the partial-array self refresh (PASR) feature enables the controller to select the amount of memory to be refreshed during self refresh. The refresh options include:

- Full array: banks 0, 1, 2, and 3
- One-half array: banks 0 and 1
- One-quarter array: bank 0
- One-eighth array: bank 0 with row address most significant bit (MSB) = 0
- One-sixteenth array: bank 0 with row address MSB = 0 and row address MSB - 1 = 0

READ and WRITE commands can still be issued to the full array during standard operation, but only the selected regions of the array will be refreshed during self refresh. Data in regions that are not selected will be lost.

Output Drive Strength

Because the device is designed for use in smaller systems that are typically point-to-point connections, an option to control the drive strength of the output buffers is provided. Drive strength should be selected based on the expected loading of the memory bus. The output driver settings are 25Ω, 37Ω, and 55Ω internal impedance for full, three-quarter, and one-half drive strengths, respectively.

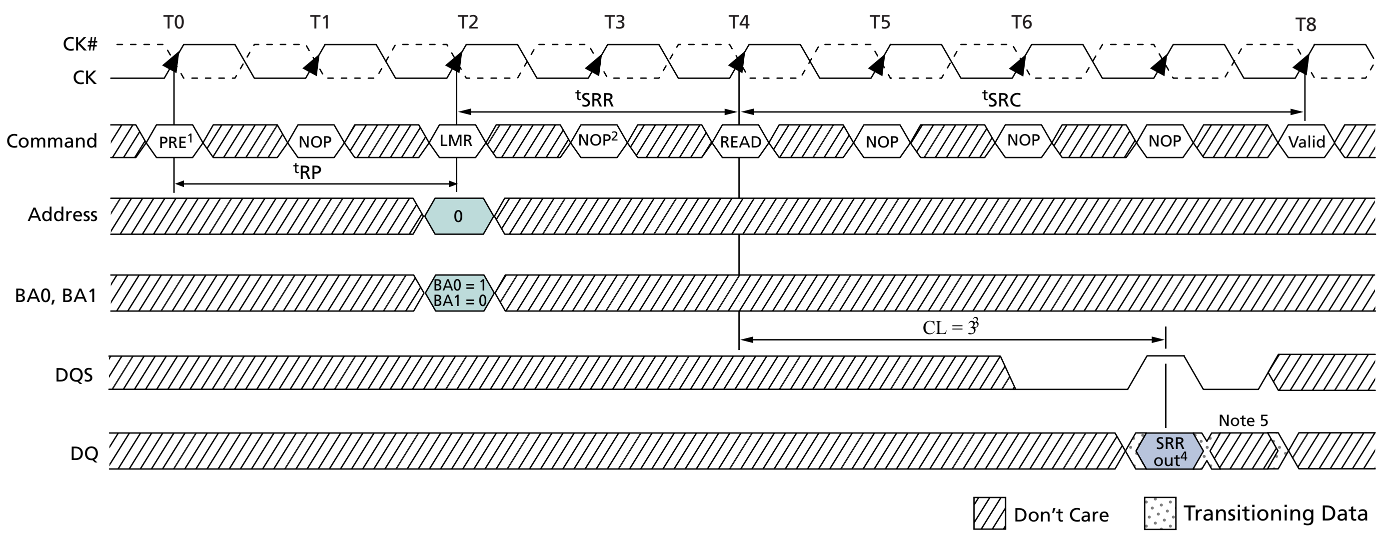
Status Read Register

The status read register (SRR) is used to read the manufacturer ID, revision ID, refresh multiplier, width type, and density of the device, as shown in Figure 27 (page 63). The SRR is read via the LOAD MODE REGISTER command with BA0 = 1 and BA1 = 0. The sequence to perform an SRR command is as follows:

1. The device must be properly initialized and in the idle or all banks precharged state.
2. Issue a LOAD MODE REGISTER command with BA[1:0] = 01 and all address pins set to 0.
3. Wait ^tSRR; only NOP or DESELECT commands are supported during the ^tSRR time.
4. Issue a READ command.
5. Subsequent commands to the device must be issued ^tSRC after the SRR READ command is issued; only NOP or DESELECT commands are supported during ^tSRC.

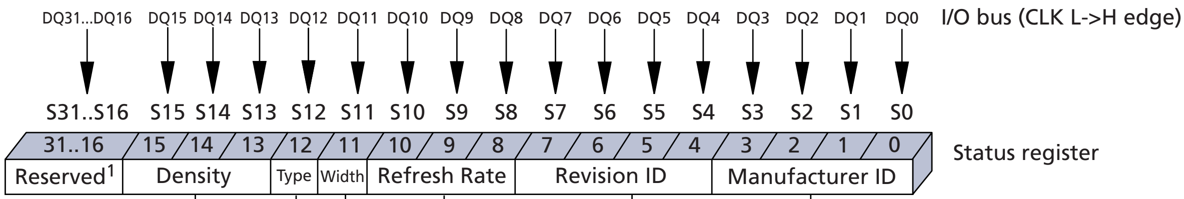
SRR output is read with a burst length of 2. SRR data is driven to the outputs on the first bit of the burst, with the output being "Don't Care" on the second bit of the burst.

Figure 26: Status Read Register Timing



Notes:
1. All banks must be idle prior to status register read.
2. NOP or DESELECT commands are required between the LMR and READ commands (^tSRR), and between the READ and the next VALID command (^tSRC).
3. CAS latency is predetermined by the programming of the mode register. CL = 3 is shown as an example only.
4. Burst length is fixed to 2 for SRR regardless of the value programmed by the mode register.
5. The second bit of the data-out burst is a "Don't Care."

Figure 27: Status Register Definition



S15	S14	S13	Density
0	0	0	128Mb
0	0	1	256Mb
0	1	0	512Mb
0	1	1	1Gb
1	0	0	2Gb
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

S12	Device Type
0	LPDDR
1	LPDDR2

S11	Device Width
0	16 bits
1	32 bits

S10	S9	S8	Refresh Multiplier[2]
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	2X
1	0	0	1X
1	0	1	Reserved
1	1	0	0.25X
1	1	1	Reserved

S3	S2	S1	S0	Manufacturer ID
0	0	0	0	Reserved
0	0	0	1	Samsung
0	0	1	0	Infineon
0	0	1	1	Elpida
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Winbond
1	0	0	1	ESMT
1	0	1	0	NVM
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Micron

S7	S6	S5	S4	Revision ID
0	0	0	0	The manufacturer's revision number starts at '0000' and increments by '0001' each time a change in the specification (AC timings or feature set), IBIS (pull-up or pull-down characteristics), or process occurs.
...	...	...	...	
X	X	X	X	

Notes:
1. Reserved bits should be set to 0 for future compatibility.
2. Refresh multiplier is based on the memory device on-board temperature sensor. Required average periodic refresh interval = ^{t}REFI × multiplier.

Bank/Row Activation

Before any READ or WRITE commands can be issued to a bank within the device, a row in that bank must be opened. This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated (see the ACTIVE Command figure). After a row is opened with the ACTIVE command, a READ or WRITE command can be issued to that row, subject to the ^{t}RCD specification.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been precharged. The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

READ Operation

READ burst operations are initiated with a READ command, as shown in Figure 16 (page 43). The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CL after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge. Figure 28 (page 66) shows general timing for each possible CL setting.

DQS is driven by the device along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble. The READ burst is considered complete when the read postamble is satisfied.

Upon completion of a burst, assuming no other commands have been initiated, the DQ will go to High-Z. A detailed explanation of ^{t}DQSQ (valid data-out skew), ^{t}QH (data-out window hold), and the valid data window is depicted in Figure 35 (page 73) and Figure 36 (page 74). A detailed explanation of ^{t}DQSCK (DQS transition skew to CK) and ^{t}AC (data-out transition skew to CK) is depicted in Figure 37 (page 75).

Data from any READ burst can be truncated by a READ or WRITE command to the same or alternate bank, by a BURST TERMINATE command, or by a PRECHARGE command to the same bank, provided that the auto precharge mode was not activated.

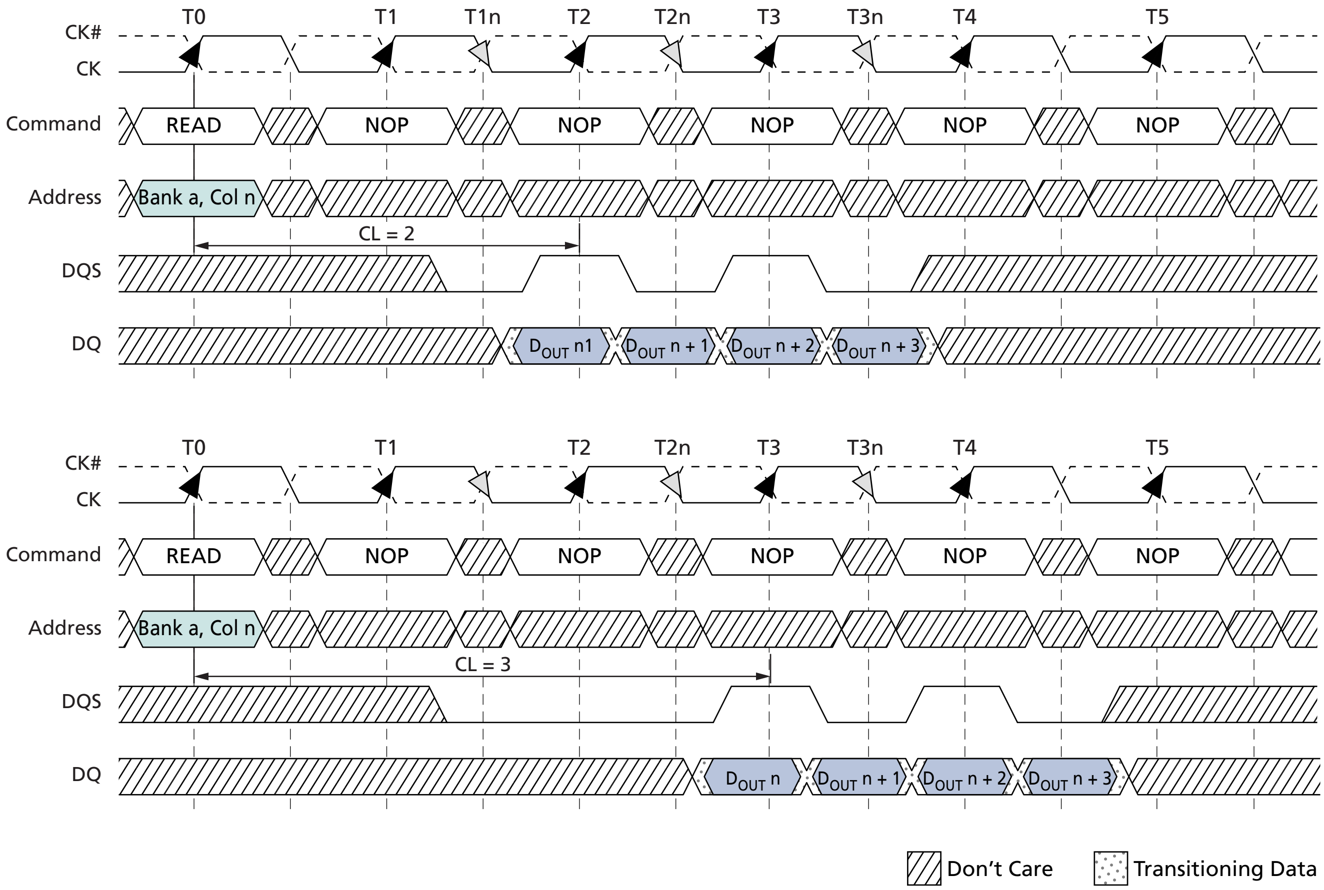
Data from any READ burst can be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst either follows the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ command should be issued *x* cycles after the first READ command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture). This is shown in Figure 29 (page 67).

A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive read data is shown in Figure 30 (page 68). Full-speed random read accesses within a page (or pages) can be performed as shown in Figure 31 (page 69).

Data from any READ burst can be truncated with a BURST TERMINATE command, as shown in Figure 32 (page 70). The BURST TERMINATE latency is equal to the READ (CAS) latency; for example, the BURST TERMINATE command should be issued *x* cycles after the READ command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture).

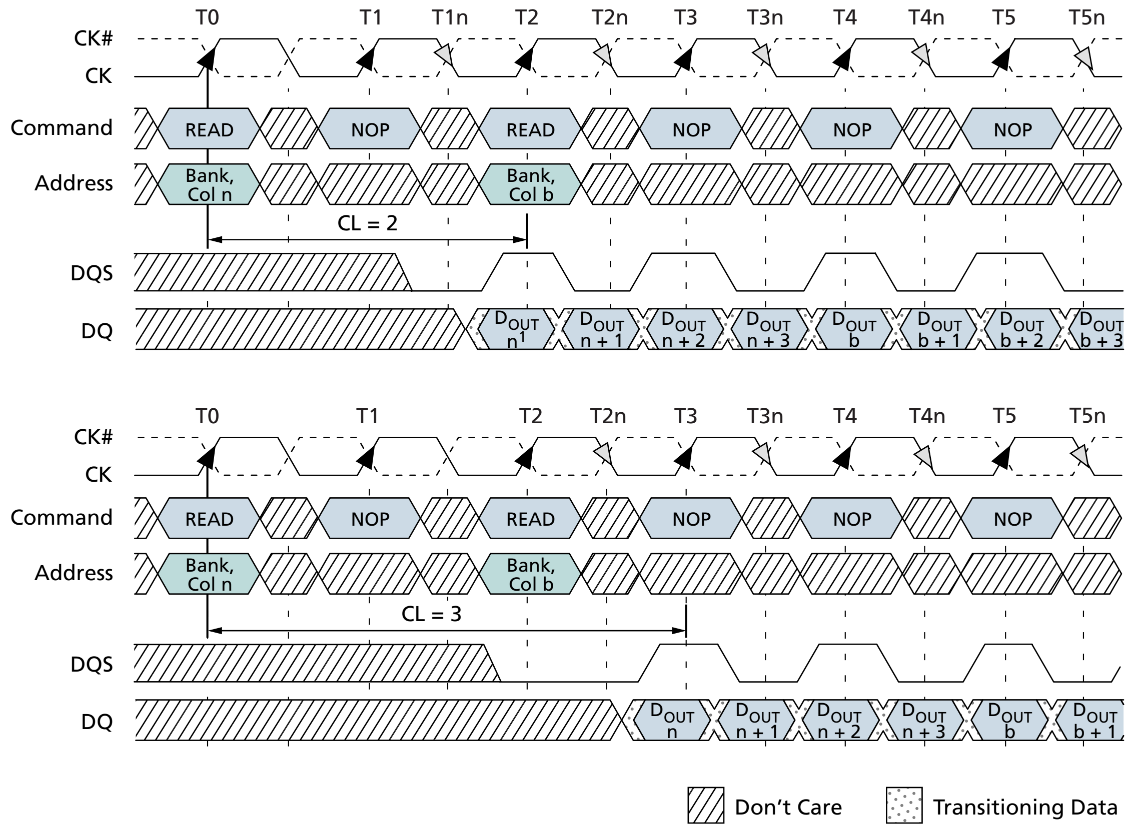
Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 33 (page 71). A READ burst can be followed by, or truncated with, a PRECHARGE command to the same bank, provided that auto precharge was not activated. The PRECHARGE command should be issued *x* cycles after the READ command, where *x* equals the number of desired data element pairs. This is shown in Figure 34 (page 72). Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met. Part of the row precharge time is hidden during the access of the last data elements.

Figure 28: READ Burst



Notes:
1. D_{OUT} *n* = data-out from column *n*.
2. BL = 4.
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

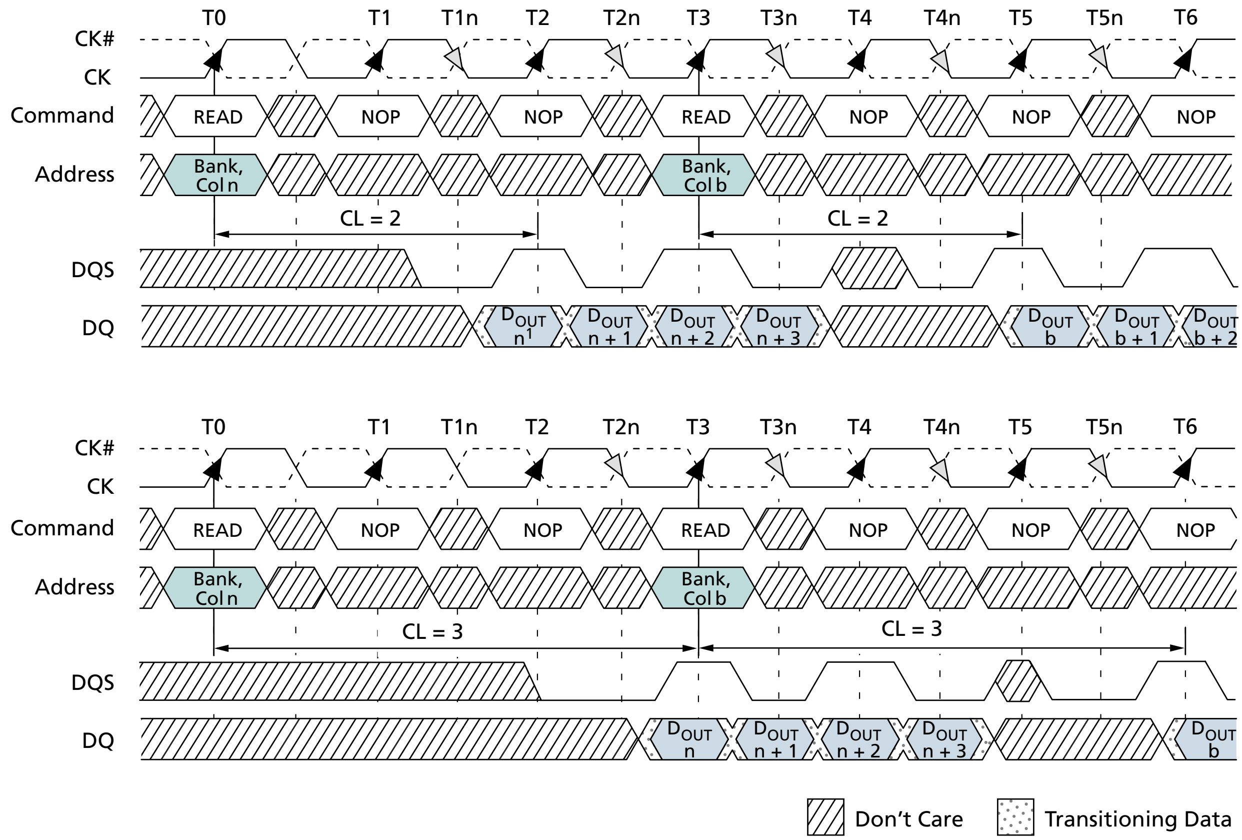
Figure 29: Consecutive READ Bursts



Notes: 1. D_{OUT} *n* (or *b*) = data-out from column *n* (or column *b*).

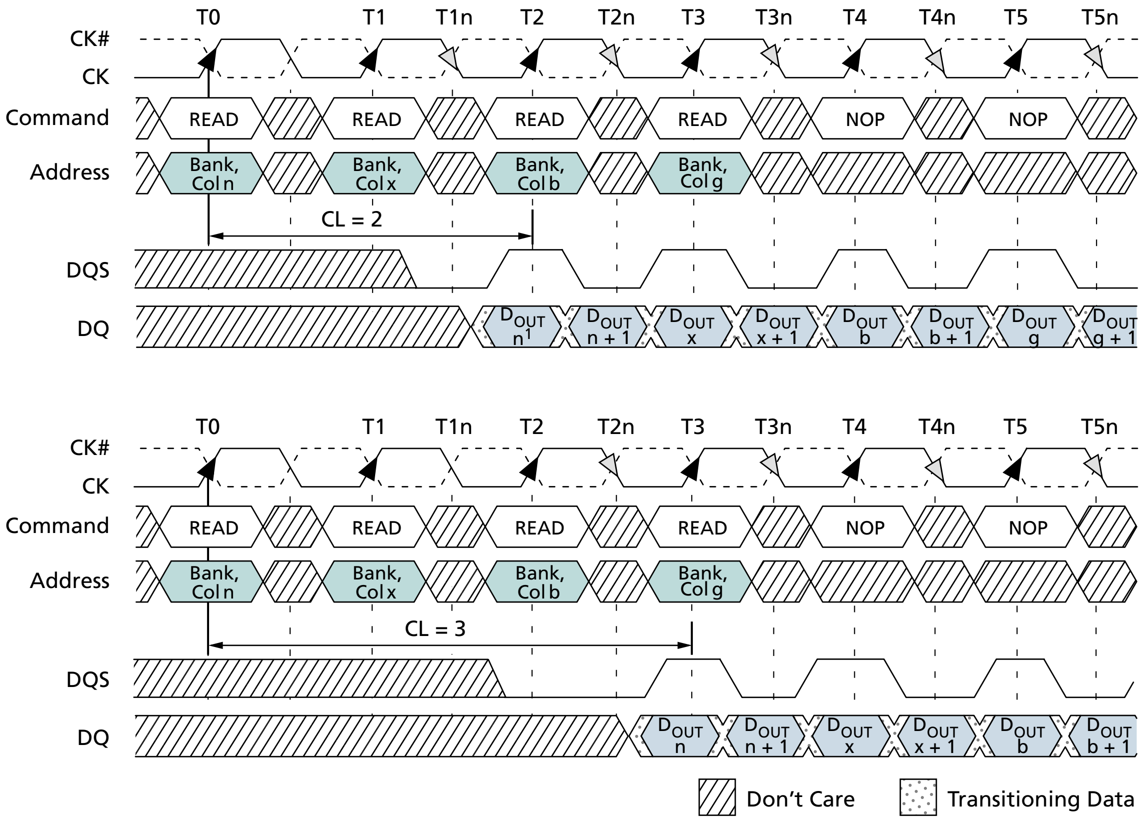
2. BL = 4, 8, or 16 (if 4, the bursts are concatenated; if 8 or 16, the second burst interrupts the first).
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
4. Example applies only when READ commands are issued to same device.

Figure 30: Nonconsecutive READ Bursts



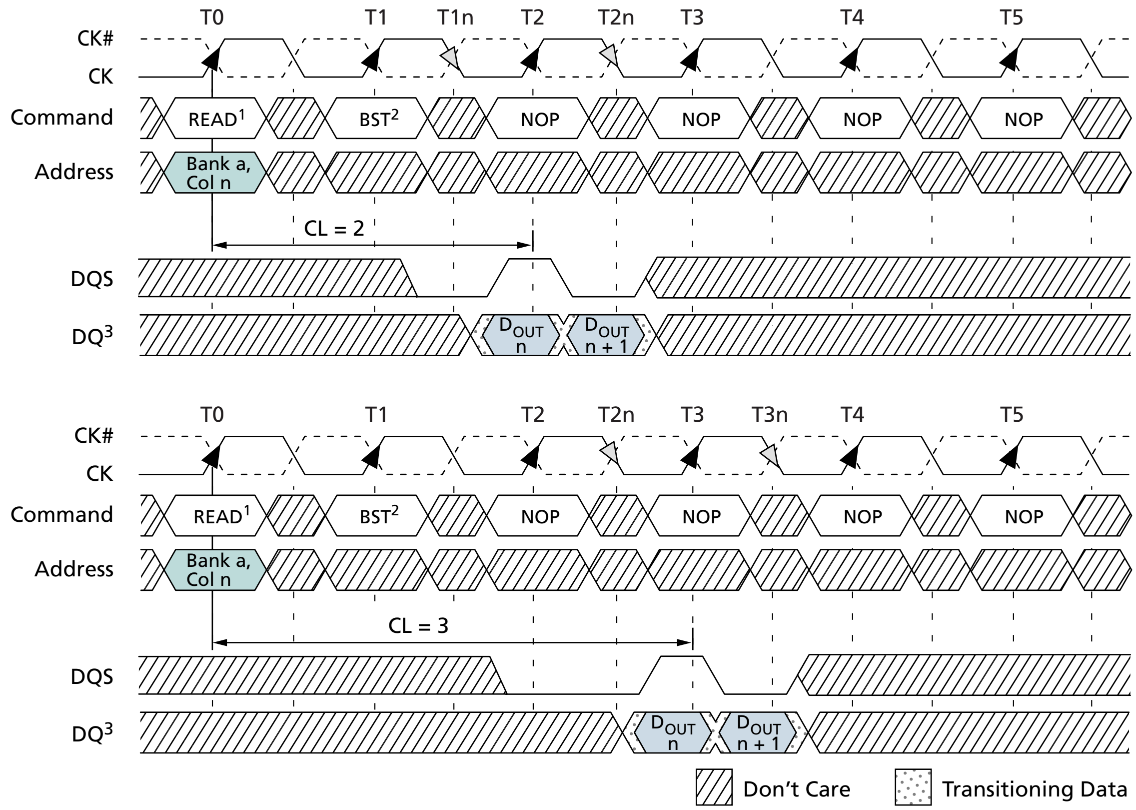
Notes:
1. D_{OUT} *n* (or *b*) = data-out from column *n* (or column *b*).
2. BL = 4, 8, or 16 (if burst is 8 or 16, the second burst interrupts the first).
3. Shown with nominal ^tAC, ^tDQSCK, and ^tDQSQ.
4. Example applies when READ commands are issued to different devices or nonconsecutive READs.

Figure 31: Random Read Accesses



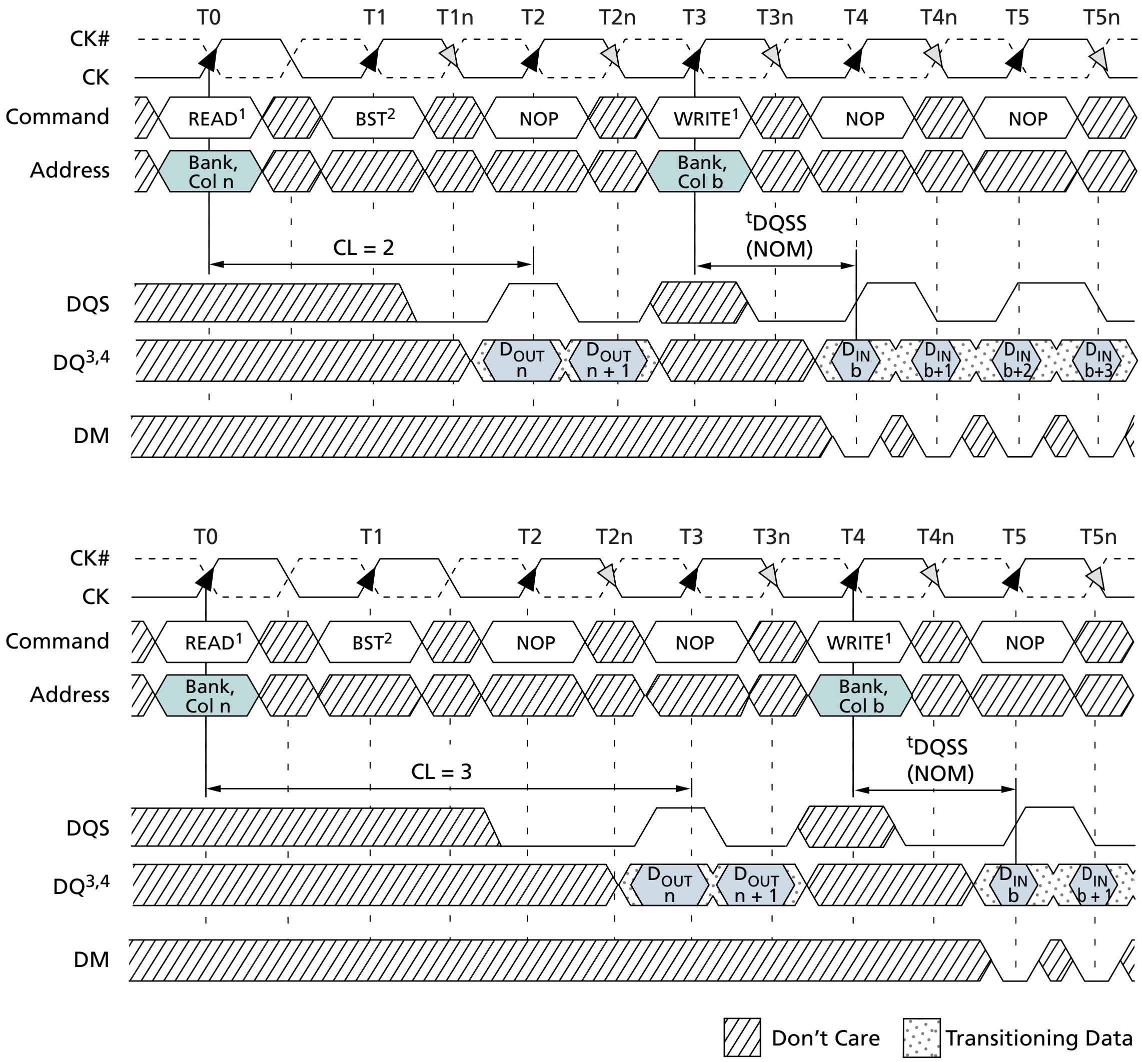
Notes:
1. D_{OUT} *n* (or *x*, *b*, *g*) = data-out from column *n* (or column *x*, column *b*, column *g*).
2. BL = 2, 4, 8, or 16 (if 4, 8, or 16, the following burst interrupts the previous).
3. READs are to an active row in any bank.
4. Shown with nominal ^tAC, ^tDQSCK, and ^tDQSQ.

Figure 32: Terminating a READ Burst



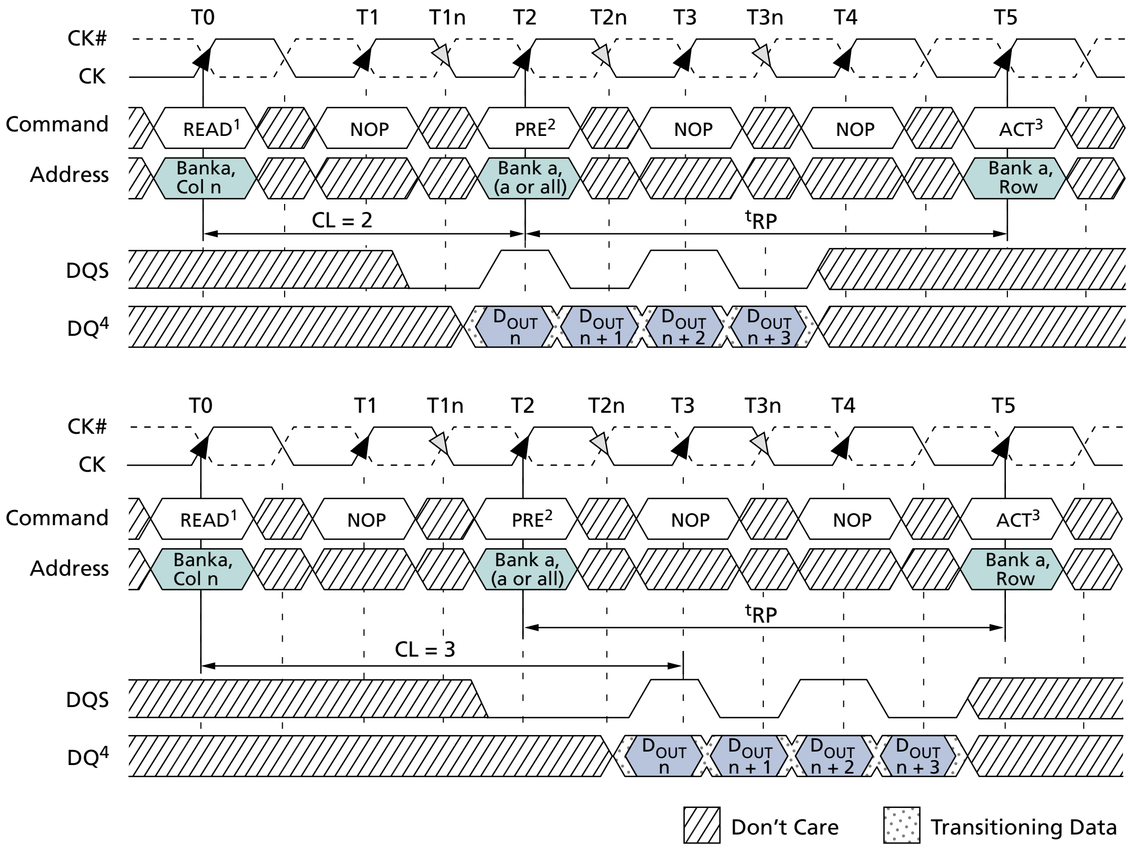
Notes:
1. BL = 4, 8, or 16.
2. BST = BURST TERMINATE command; page remains open.
3. D_{OUT} *n* = data-out from column *n*.
4. Shown with nominal ^tAC, ^tDQSCK, and ^tDQSQ.
5. CKE = HIGH.

Figure 33: READ-to-WRITE



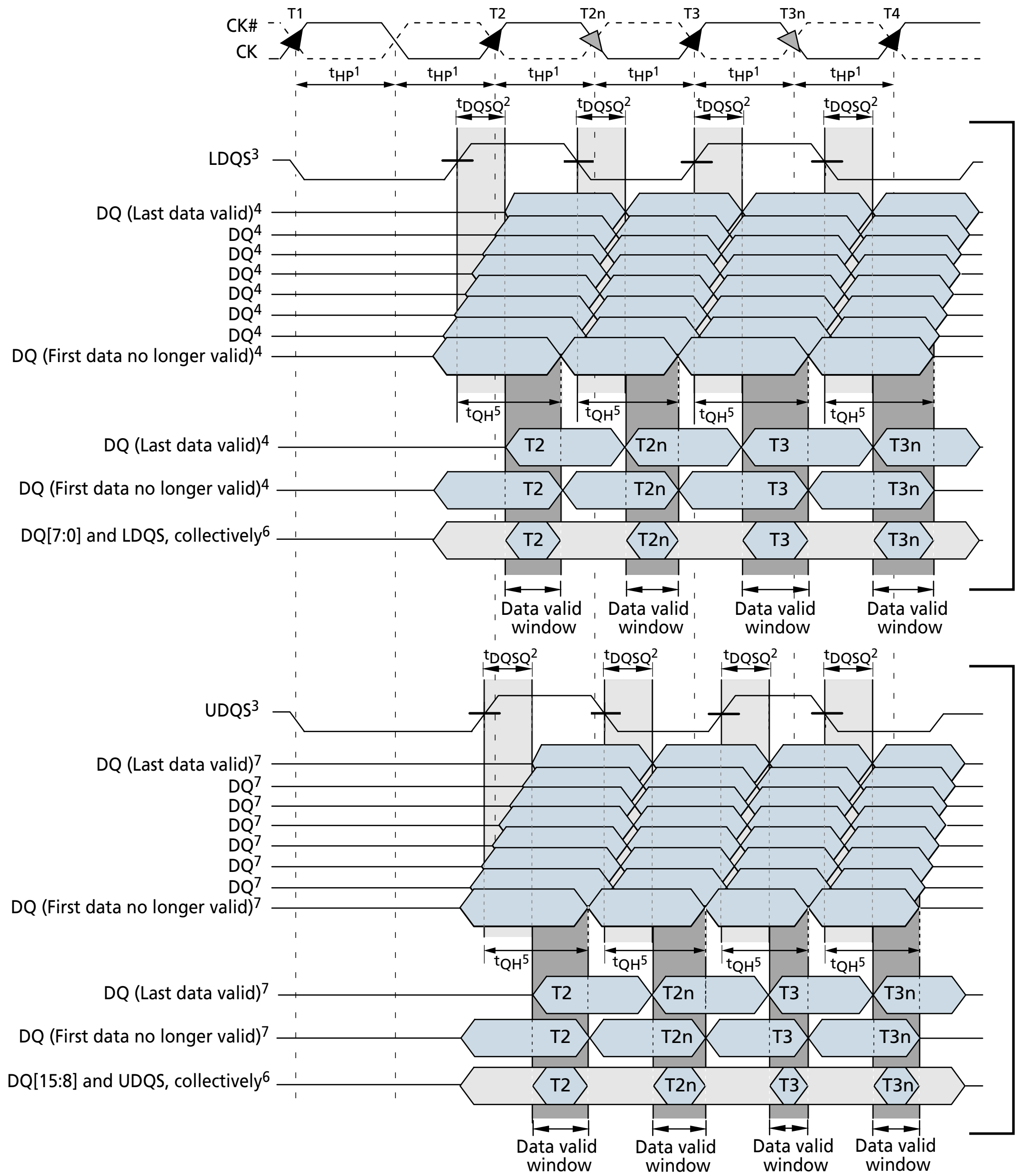
Notes:
1. BL = 4 in the cases shown (applies for bursts of 8 and 16 as well; if BL = 2, the BST command shown can be NOP).
2. BST = BURST TERMINATE command; page remains open.
3. D_{OUT} *n* = data-out from column *n*.
4. D_{IN} *b* = data-in from column *b*.
5. Shown with nominal ^tAC, ^tDQSCK, and ^tDQSQ.
6. CKE = HIGH.

Figure 34: READ-to-PRECHARGE



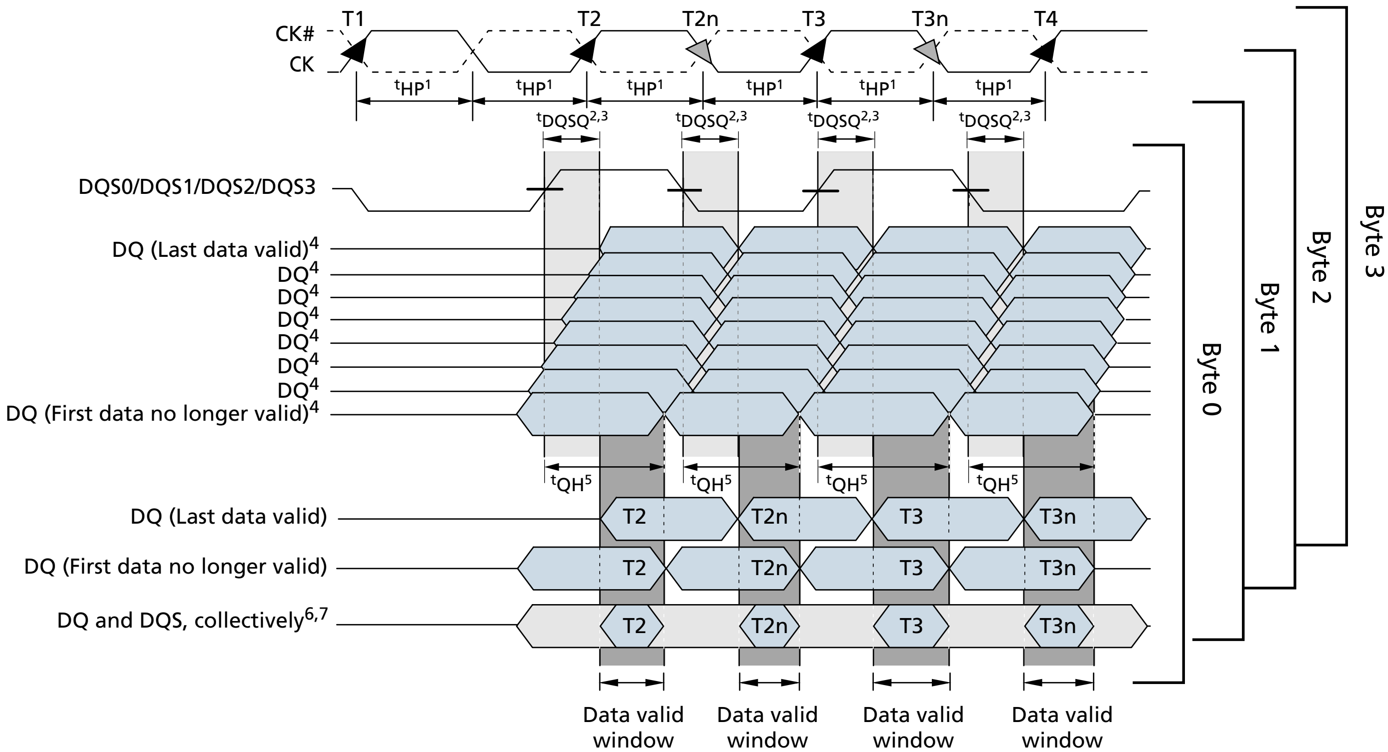
Notes:
1. BL = 4, or an interrupted burst of 8 or 16.
2. PRE = PRECHARGE command.
3. ACT = ACTIVE command.
4. D_{OUT} *n* = data-out from column *n*.
5. Shown with nominal ^tAC, ^tDQSCK, and ^tDQSQ.
6. READ-to-PRECHARGE equals 2 clocks, which enables 2 data pairs of data-out.
7. A READ command with auto precharge enabled, provided ^tRAS (MIN) is met, would cause a precharge to be performed at *x* number of clock cycles after the READ command, where *x* = BL/2.

Figure 35: Data Output Timing – ^tDQSQ, ^tQH, and Data Valid Window (x16)



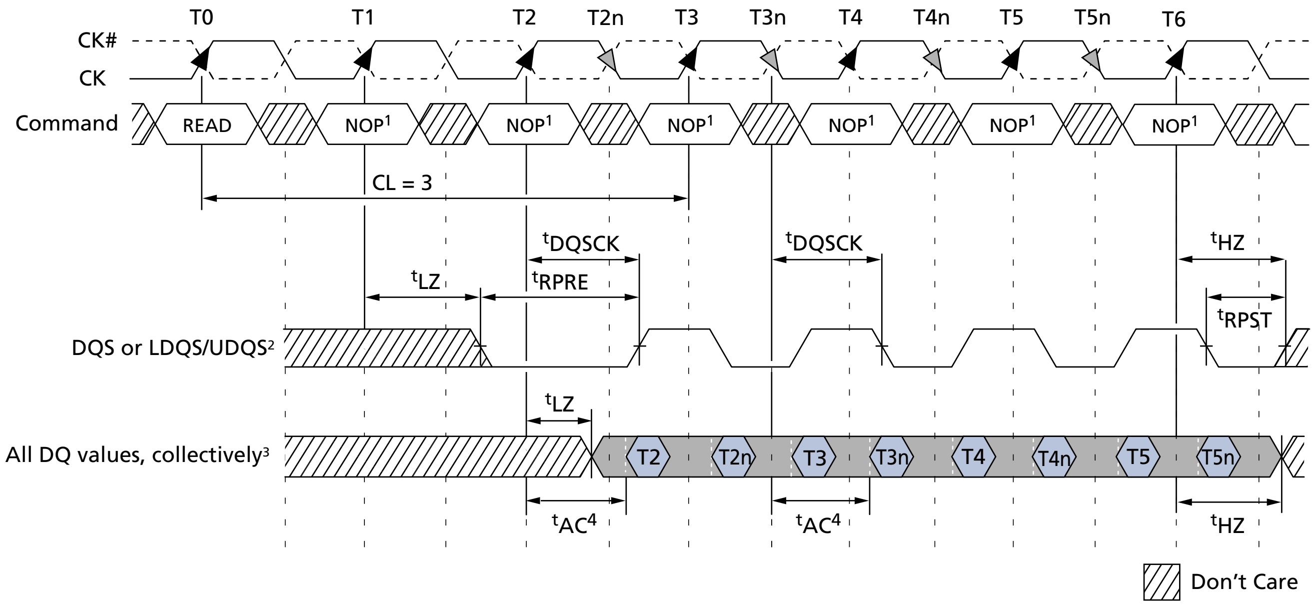
Notes:
1. ^tHP is the lesser of ^tCL or ^tCH clock transition collectively when a bank is active.
2. ^tDQSQ is derived at each DQS clock edge and is not cumulative over time and begins with DQS transition and ends with the last valid DQ transition.
3. DQ transitioning after DQS transitions define the ^tDQSQ window. LDQS defines the lower byte and UDQS defines the upper byte.
4. DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, or DQ7.
5. ^tQH is derived from ^tHP: $^tQH = {}^tHP - {}^tQHS$.
6. The data valid window is derived for each DQS transitions and is defined as $^tQH - {}^tDQSQ$.
7. DQ8, DQ9, DQ10, DQ11, DQ12, DQ13, DQ14, or DQ15.

Figure 36: Data Output Timing – ^tDQSQ, ^tQH, and Data Valid Window (x32)



Notes:
1. ^tHP is the lesser of ^tCL or ^tCH clock transition collectively when a bank is active.
2. DQ transitioning after DQS transitions define the ^tDQSQ window.
3. ^tDQSQ is derived at each DQS clock edge and is not cumulative over time; it begins with DQS transition and ends with the last valid DQ transition.
4. Byte 0 is DQ[7:0], byte 1 is DQ[15:8], byte 2 is DQ[23:16], byte 3 is DQ[31:24].
5. ^tQH is derived from ^tHP: $^tQH = {}^tHP - {}^tQHS$.
6. The data valid window is derived for each DQS transition and is $^tQH - {}^tDQSQ$.
7. DQ[7:0] and DQS0 for byte 0; DQ[15:8] and DQS1 for byte 1; DQ[23:16] and DQS2 for byte 2; DQ[31:23] and DQS3 for byte 3.

Figure 37: Data Output Timing – ^{t}AC and ^{t}DQSCK



Notes:
1. Commands other than NOP can be valid during this cycle.
2. DQ transitioning after DQS transitions define ^{t}DQSQ window.
3. All DQ must transition by ^{t}DQSQ after DQS transitions, regardless of ^{t}AC.
4. ^{t}AC is the DQ output window relative to CK and is the long-term component of DQ skew.

WRITE Operation

WRITE bursts are initiated with a WRITE command, as shown in Figure 17 (page 44). The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the WRITE commands used in the following illustrations, auto precharge is disabled. Basic data input timing is shown in Figure 38 (page 77) (this timing applies to all WRITE operations).

Input data appearing on the data bus is written to the memory array subject to the state of data mask (DM) inputs coincident with the data. If DM is registered LOW, the corresponding data will be written; if DM is registered HIGH, the corresponding data will be ignored, and the write will not be executed to that byte/column location. DM operation is illustrated in Figure 39 (page 78).

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state of DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state of DQS following the last data-in element is known as the write postamble. The WRITE burst is complete when the write postamble and ^{t}WR or ^{t}WTR are satisfied.

The time between the WRITE command and the first corresponding rising edge of DQS (^{t}DQSS) is specified with a relatively wide range (75%–125% of one clock cycle). All WRITE diagrams show the nominal case. Where the two extreme cases (that is, ^{t}DQSS [MIN] and ^{t}DQSS [MAX]) might not be obvious, they have also been included. Figure 40 (page 79) shows the nominal case and the extremes of ^{t}DQSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst can be concatenated with or truncated by a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new WRITE command should be issued x cycles after the first WRITE command, where x equals the number of desired data element pairs (pairs are required by the $2n$-prefetch architecture).

Figure 41 (page 80) shows concatenated bursts of 4. An example of nonconsecutive WRITEs is shown in Figure 42 (page 80). Full-speed random write accesses within a page or pages can be performed, as shown in Figure 43 (page 81).

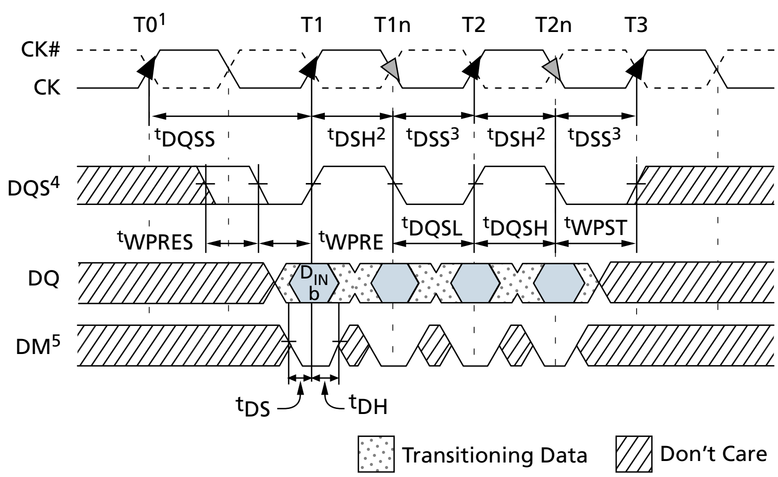
Data for any WRITE burst can be followed by a subsequent READ command. To follow a WRITE without truncating the WRITE burst, ^{t}WTR should be met, as shown in Figure 44 (page 82).

Data for any WRITE burst can be truncated by a subsequent READ command, as shown in Figure 45 (page 83). Note that only the data-in pairs that are registered prior to the ^{t}WTR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure 46 (page 84).

Data for any WRITE burst can be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the WRITE burst, ^{t}WR should be met, as shown in Figure 47 (page 85).

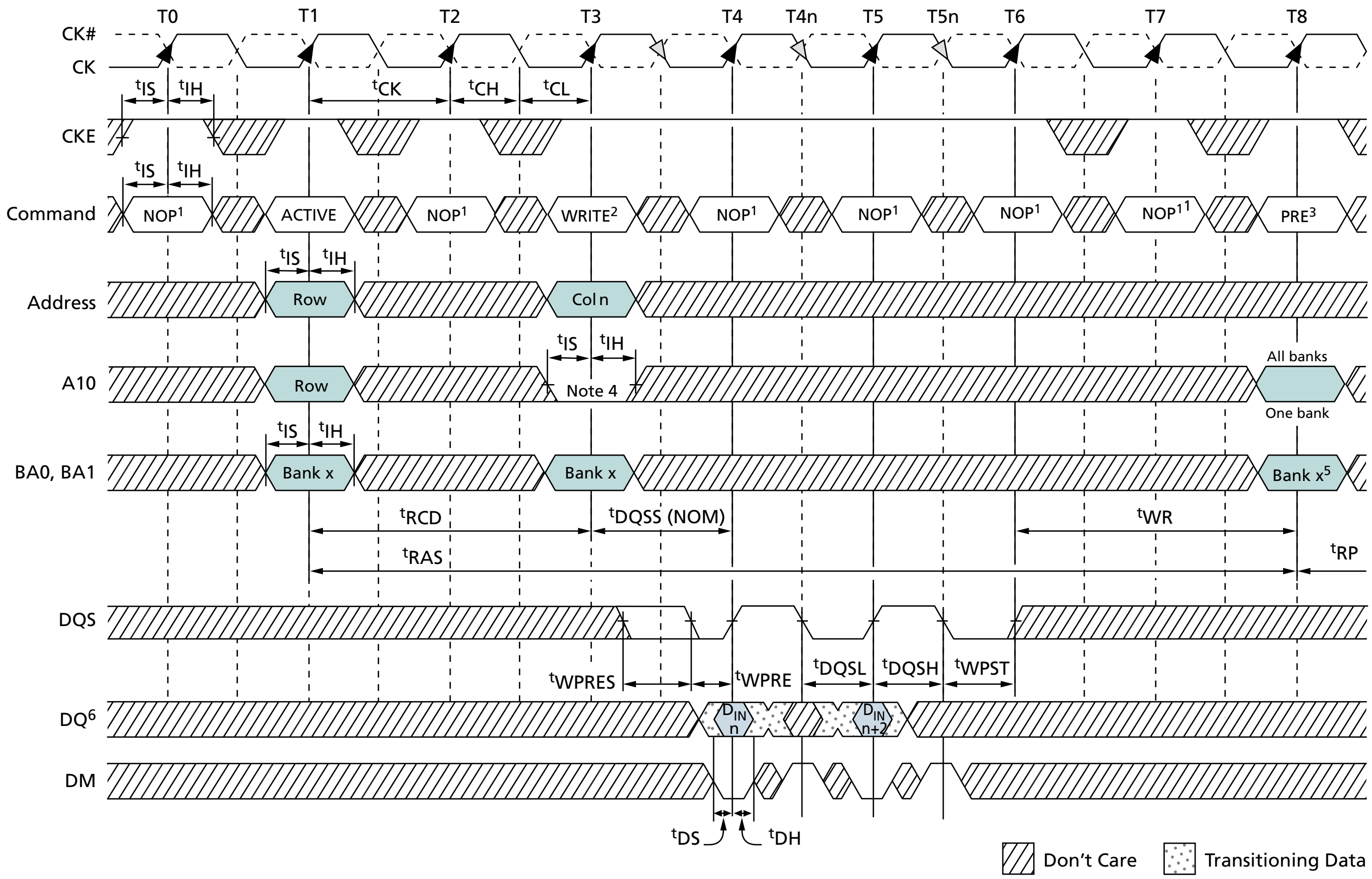
Data for any WRITE burst can be truncated by a subsequent PRECHARGE command, as shown in Figure 48 (page 86) and Figure 49 (page 87). Note that only the data-in pairs that are registered prior to the ^{t}WR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure 48 (page 86) and Figure 49 (page 87). After the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met.

Figure 38: Data Input Timing



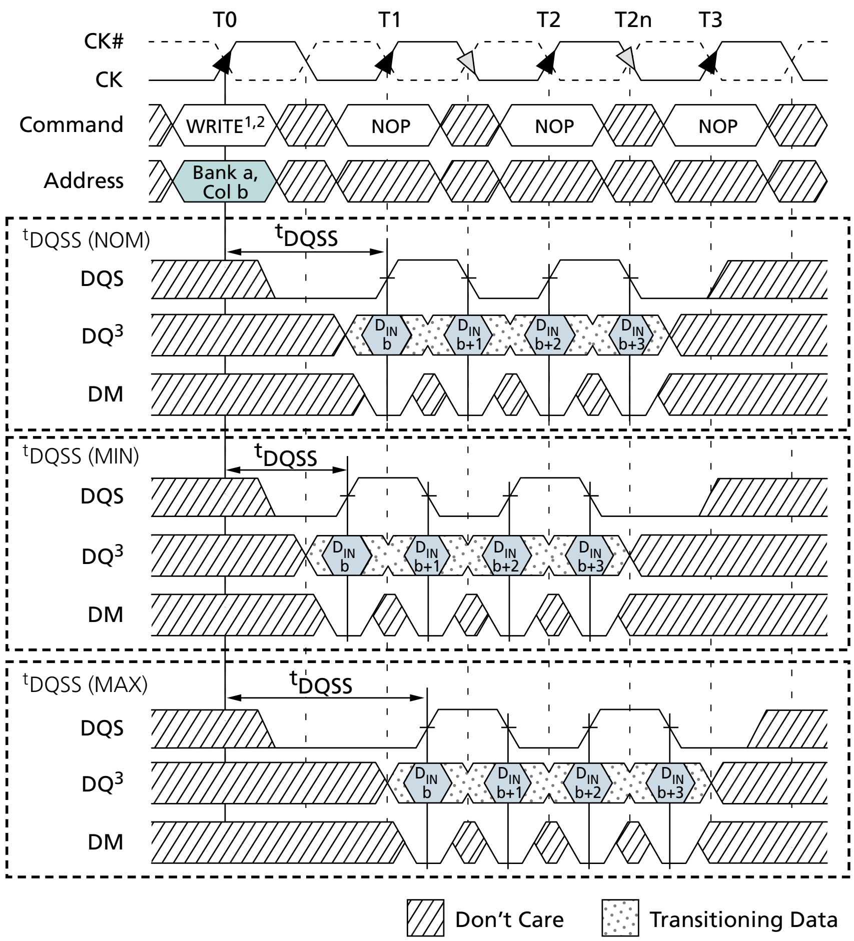
Notes:
1. WRITE command issued at T0.
2. ^{t}DSH (MIN) generally occurs during ^{t}DQSS (MIN).
3. ^{t}DSS (MIN) generally occurs during ^{t}DQSS (MAX).
4. For x16, LDQS controls the lower byte; UDQS controls the upper byte. For x32, DQS0 controls DQ[7:0], DQS1 controls DQ[15:8], DQS2 controls DQ[23:16], and DQS3 controls DQ[31:24].
5. For x16, LDM controls the lower byte; UDM controls the upper byte. For x32, DM0 controls DQ[7:0], DM1 controls DQ[15:8], DM2 controls DQ[23:16], and DM3 controls DQ[31:24].

Figure 39: Write – DM Operation



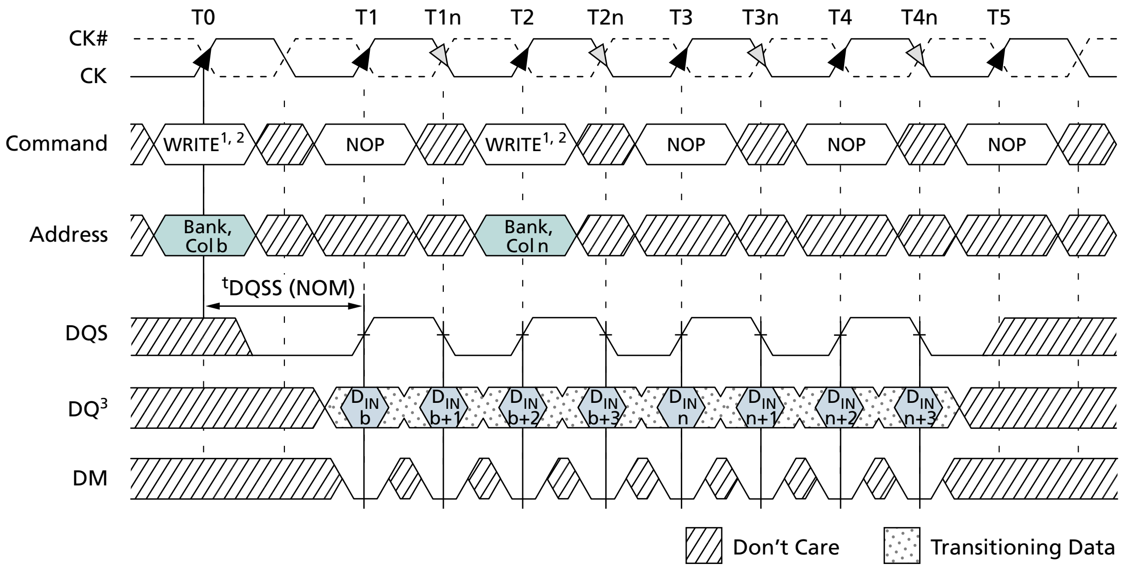
Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4 in the case shown.
3. PRE = PRECHARGE.
4. Disable auto precharge.
5. Bank *x* at T8 is "Don't Care" if A10 is HIGH at T8.
6. D_{IN} *n* = data-in from column *n*.

Figure 40: WRITE Burst



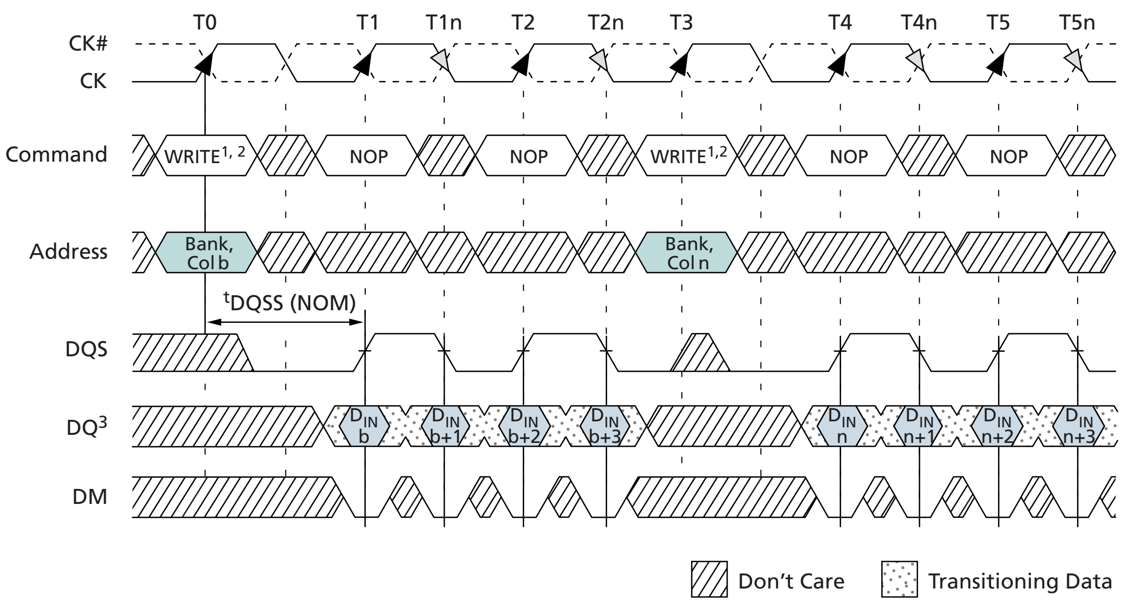
Notes:
1. An uninterrupted burst of 4 is shown.
2. A10 is LOW with the WRITE command (auto precharge is disabled).
3. D_{IN} *b* = data-in for column *b*.

Figure 41: Consecutive WRITE-to-WRITE



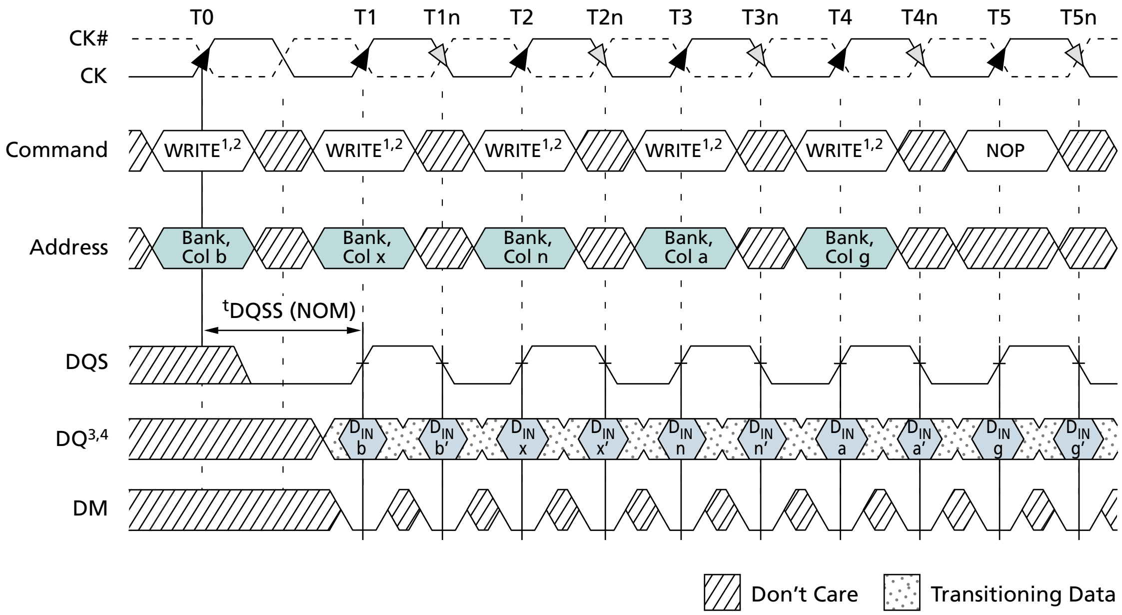
Notes:
1. Each WRITE command can be to any bank.
2. An uninterrupted burst of 4 is shown.
3. D_{IN} *b* (*n*) = data-in for column *b* (*n*).

Figure 42: Nonconsecutive WRITE-to-WRITE



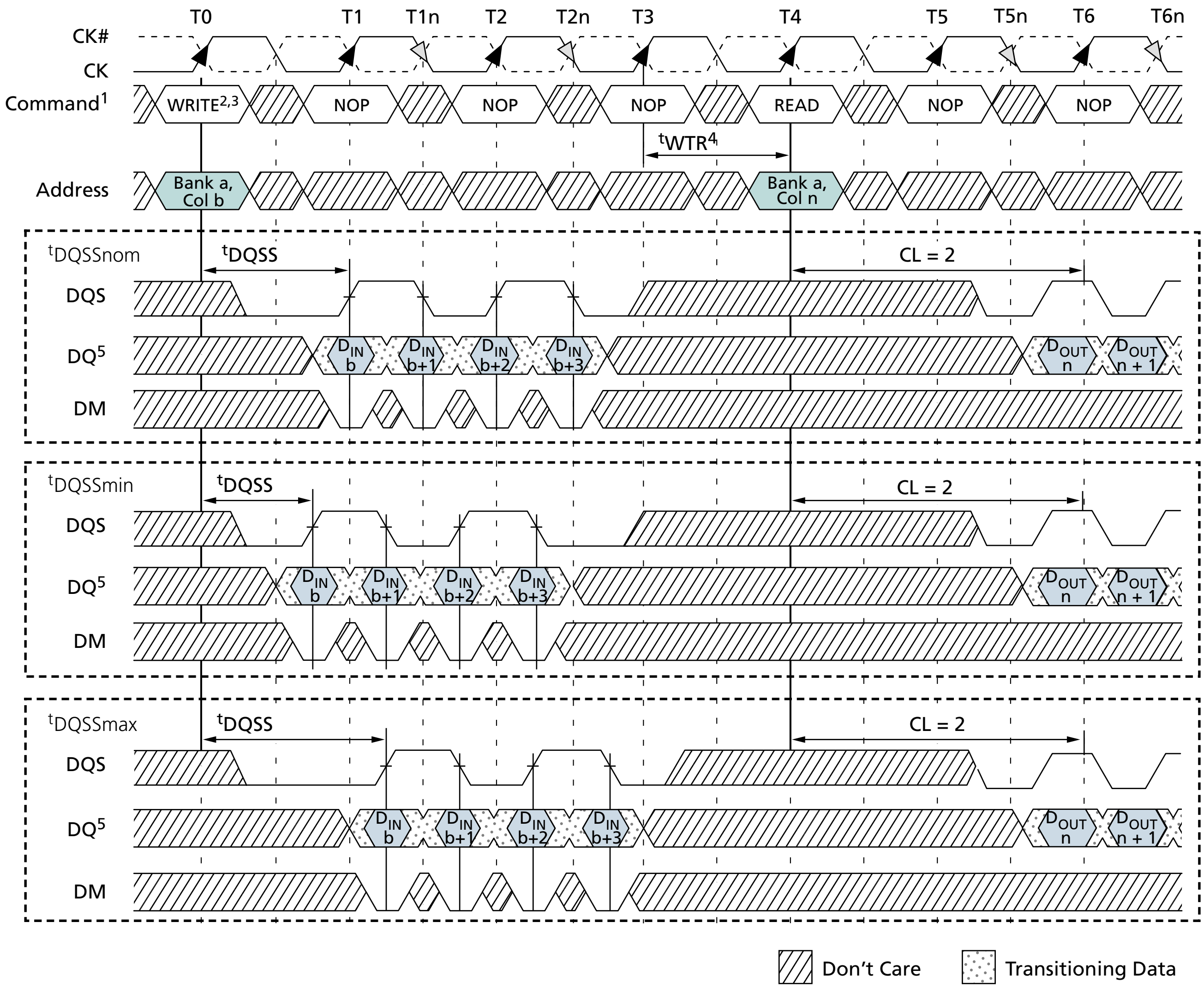
Notes:
1. Each WRITE command can be to any bank.
2. An uninterrupted burst of 4 is shown.
3. D_{IN} *b* (*n*) = data-in for column *b* (*n*).

Figure 43: Random WRITE Cycles



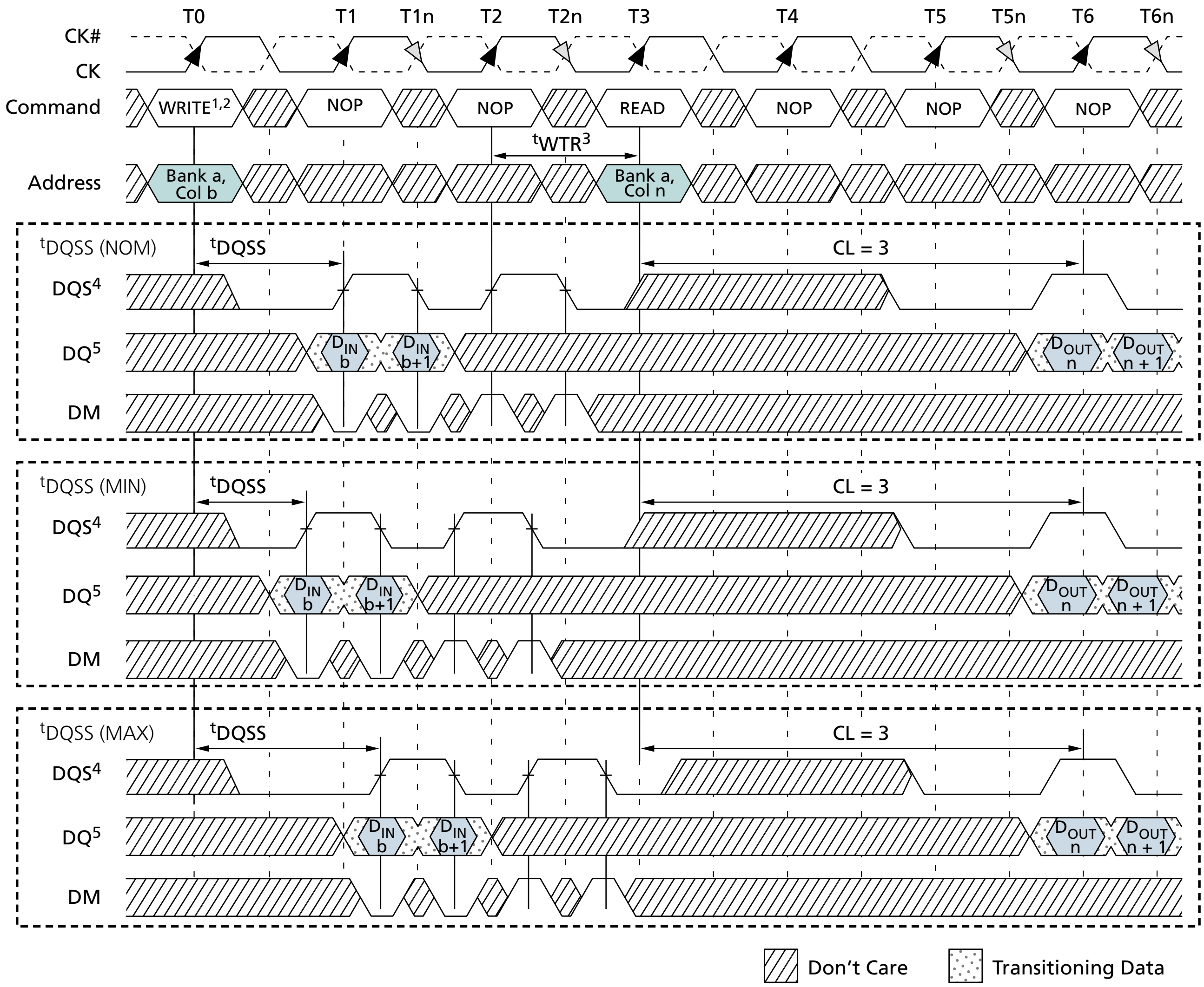
Notes:
1. Each WRITE command can be to any bank.
2. Programmed BL = 2, 4, 8, or 16 in cases shown.
3. D_{IN} *b* (*or x*, *n*, *a*, *g*) = data-in for column *b* (or *x*, *n*, *a*, *g*).
4. b' (or *x, n, a, g*) = the next data-in following D_{IN} *b* (*x, n, a, g*) according to the programmed burst order.

Figure 44: WRITE-to-READ – Uninterrupting



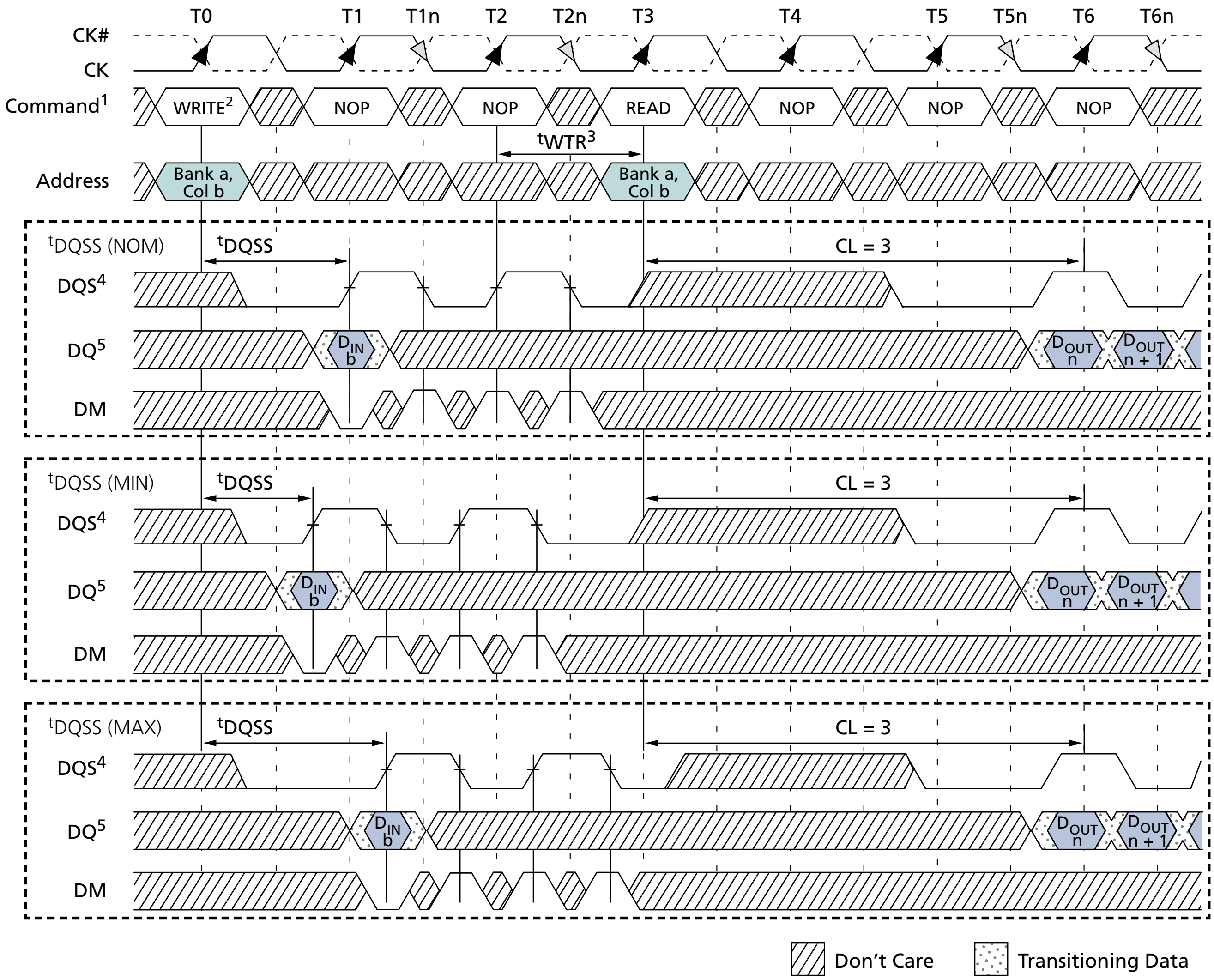
Notes:
1. The READ and WRITE commands are to the same device. However, the READ and WRITE commands may be to different devices, in which case tWTR is not required and the READ command could be applied earlier.
2. A10 is LOW with the WRITE command (auto precharge is disabled).
3. An uninterrupted burst of 4 is shown.
4. tWTR is referenced from the first positive CK edge after the last data-in pair.
5. D_{IN} *b* = data-in for column *b*; D_{OUT} *n* = data-out for column *n*.

Figure 45: WRITE-to-READ – Interrupting



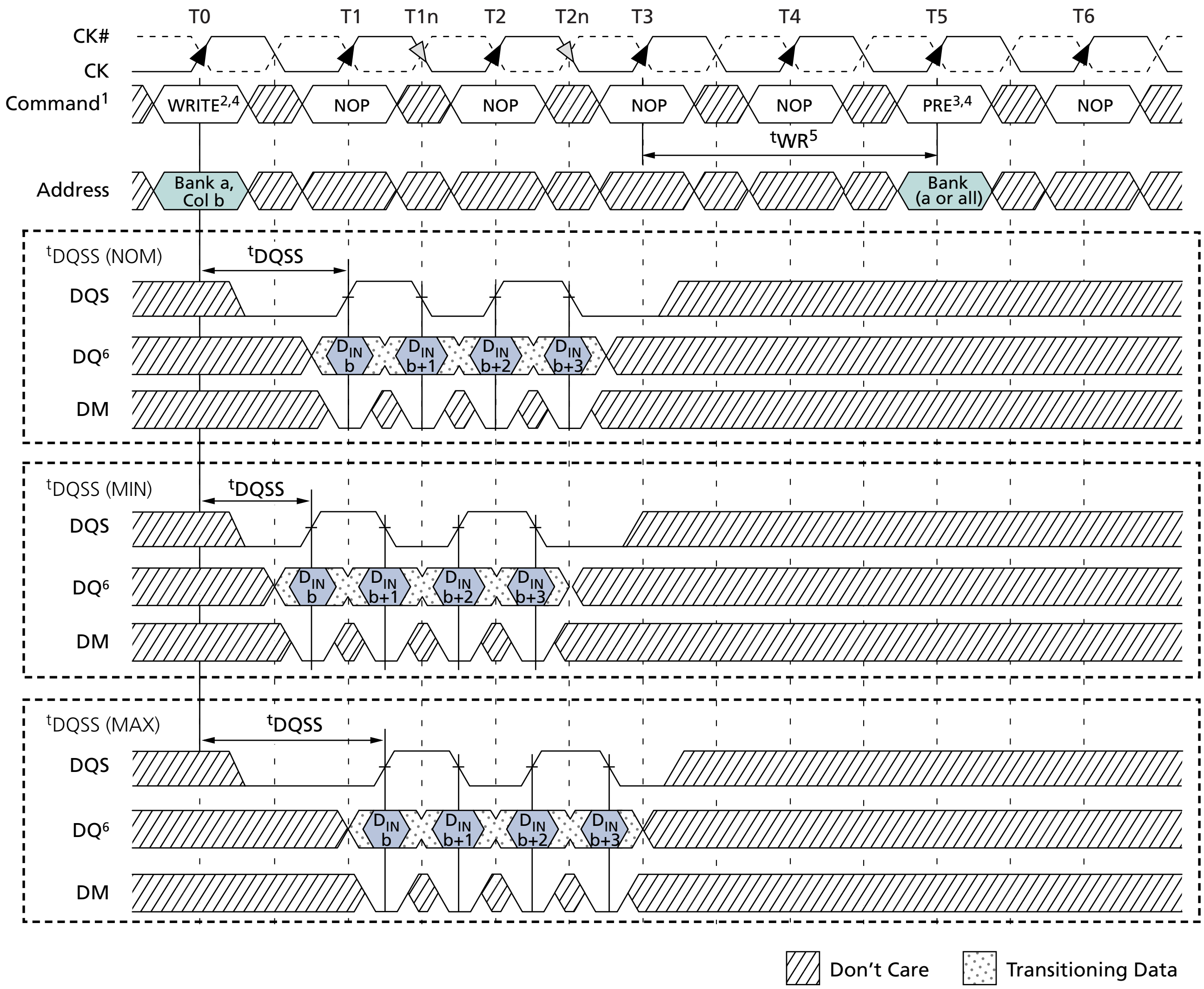
Notes:
1. An interrupted burst of 4 is shown; 2 data elements are written.
2. A10 is LOW with the WRITE command (auto precharge is disabled).
3. ^{t}WTR is referenced from the first positive CK edge after the last data-in pair.
4. DQS is required at T2 and T2n (nominal case) to register DM.
5. D_{IN} *b* = data-in for column *b*; D_{OUT} *n* = data-out for column *n*.

Figure 46: WRITE-to-READ – Odd Number of Data, Interrupting



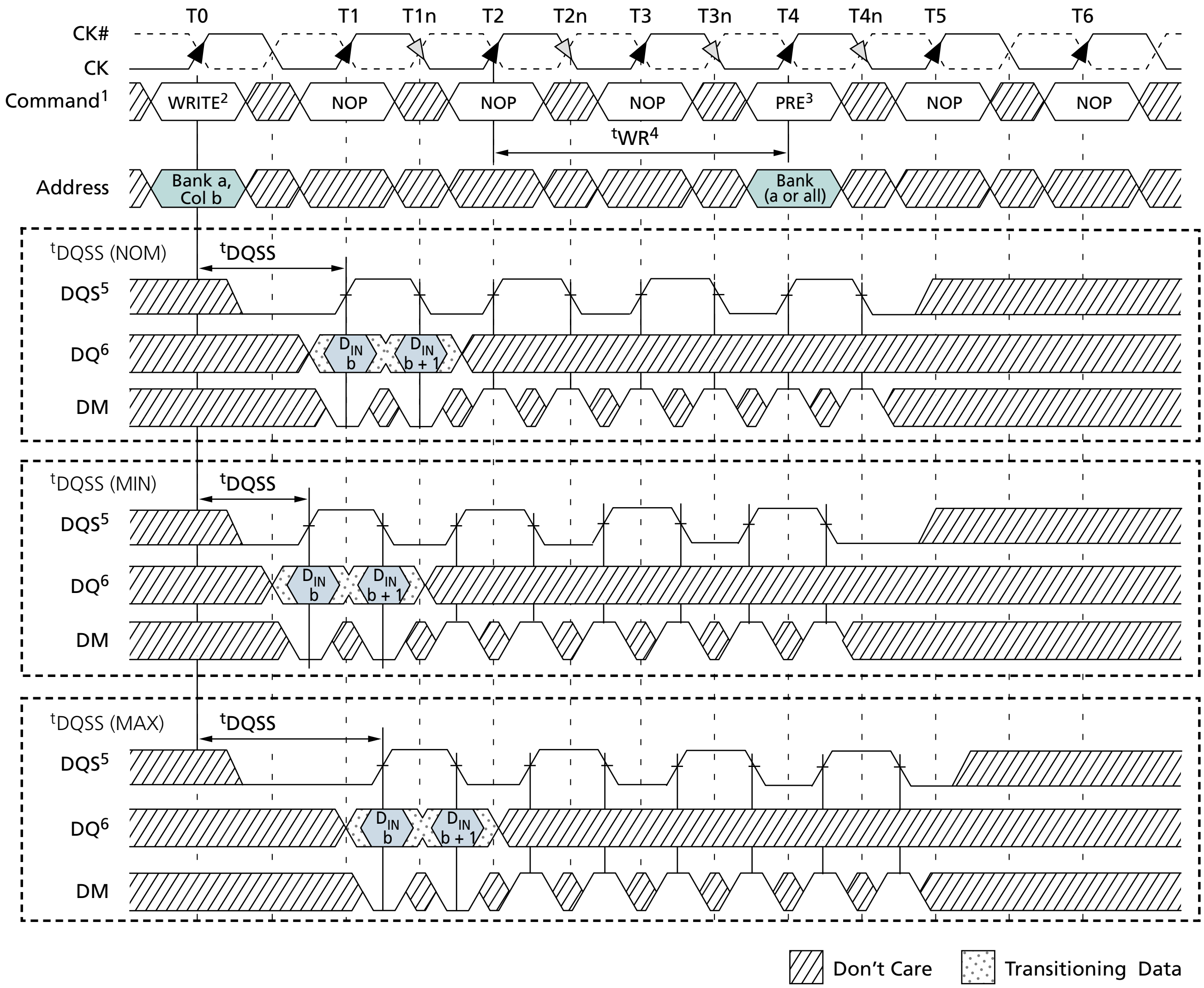
Notes:
1. An interrupted burst of 4 is shown; 1 data element is written, 3 are masked.
2. A10 is LOW with the WRITE command (auto precharge is disabled).
3. ^{t}WTR is referenced from the first positive CK edge after the last data-in pair.
4. DQS is required at T2 and T2n (nominal case) to register DM.
5. D_{IN} *b* = data-in for column *b*; D_{OUT} *n* = data-out for column *n*.

Figure 47: WRITE-to-PRECHARGE – Uninterrupting



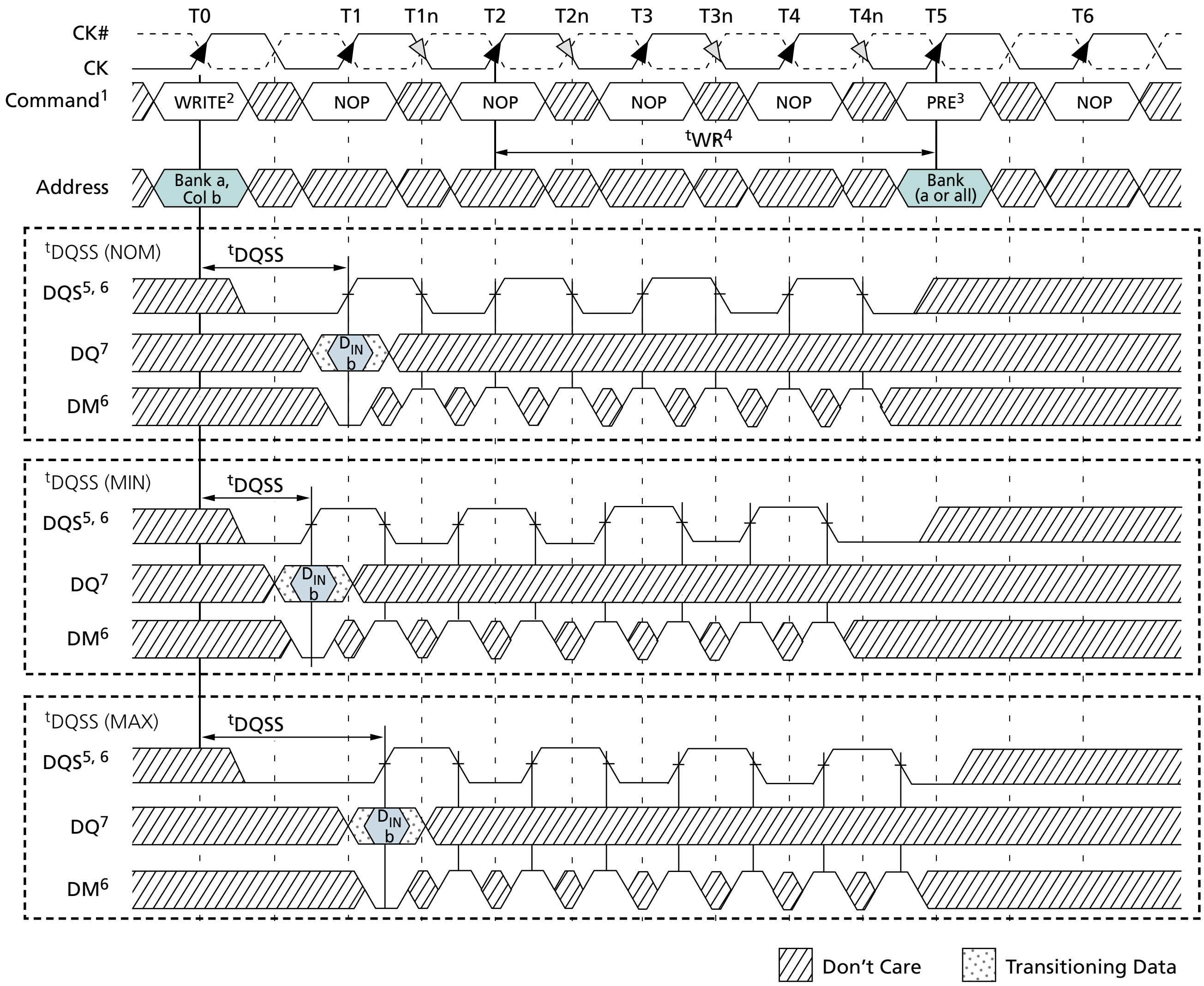
Notes:
1. An uninterrupted burst 4 of is shown.
2. A10 is LOW with the WRITE command (auto precharge is disabled).
3. PRE = PRECHARGE.
4. The PRECHARGE and WRITE commands are to the same device. However, the PRECHARGE and WRITE commands can be to different devices; in this case, ^{t}WR is not required and the PRECHARGE command can be applied earlier.
5. ^{t}WR is referenced from the first positive CK edge after the last data-in pair.
6. D_{IN} *b* = data-in for column *b*.

Figure 48: WRITE-to-PRECHARGE – Interrupting



Notes:
1. An interrupted burst of 8 is shown; two data elements are written.
2. A10 is LOW with the WRITE command (auto precharge is disabled).
3. PRE = PRECHARGE.
4. ^{t}WR is referenced from the first positive CK edge after the last data-in pair.
5. DQS is required at T4 and T4n to register DM.
6. D_{IN} *b* = data-in for column *b*.

Figure 49: WRITE-to-PRECHARGE – Odd Number of Data, Interrupting



Notes:
1. An interrupted burst of 8 is shown; one data element is written.
2. A10 is LOW with the WRITE command (auto precharge is disabled).
3. PRE = PRECHARGE.
4. ^{t}WR is referenced from the first positive CK edge after the last data-in pair.
5. DQS is required at T4 and T4n to register DM.
6. If a burst of 4 is used, DQS and DM are not required at T3, T3n, T4, and T4n.
7. D_{IN} *b* = data-in for column *b*.

PRECHARGE Operation

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (^tRP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks will be precharged, and in the case where only one bank is precharged (A10 = LOW), inputs BA0 and BA1 select the bank. When all banks are precharged (A10 = HIGH), inputs BA0 and BA1 are treated as "Don't Care." After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

Auto Precharge

Auto precharge is a feature that performs the same individual bank PRECHARGE function described previously, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is nonpersistent; it is either enabled or disabled for each individual READ or WRITE command.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This earliest valid stage is determined as if an explicit PRECHARGE command was issued at the earliest possible time without violating ^tRAS (MIN), as described for each burst type in Table 19 (page 49). The READ with auto precharge enabled state or the WRITE with auto precharge enabled state can each be broken into two parts: the access period and the precharge period. The access period starts with registration of the command and ends where ^tRP (the precharge period) begins. For READ with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled, followed by the earliest possible PRECHARGE command that still accesses all the data in the burst. For WRITE with auto precharge, the precharge period begins when ^tWR ends, with ^tWR measured as if auto precharge was disabled. In addition, during a WRITE with auto precharge, at least one clock is required during ^tWR time. During the precharge period, the user must not issue another command to the same bank until ^tRP is satisfied.

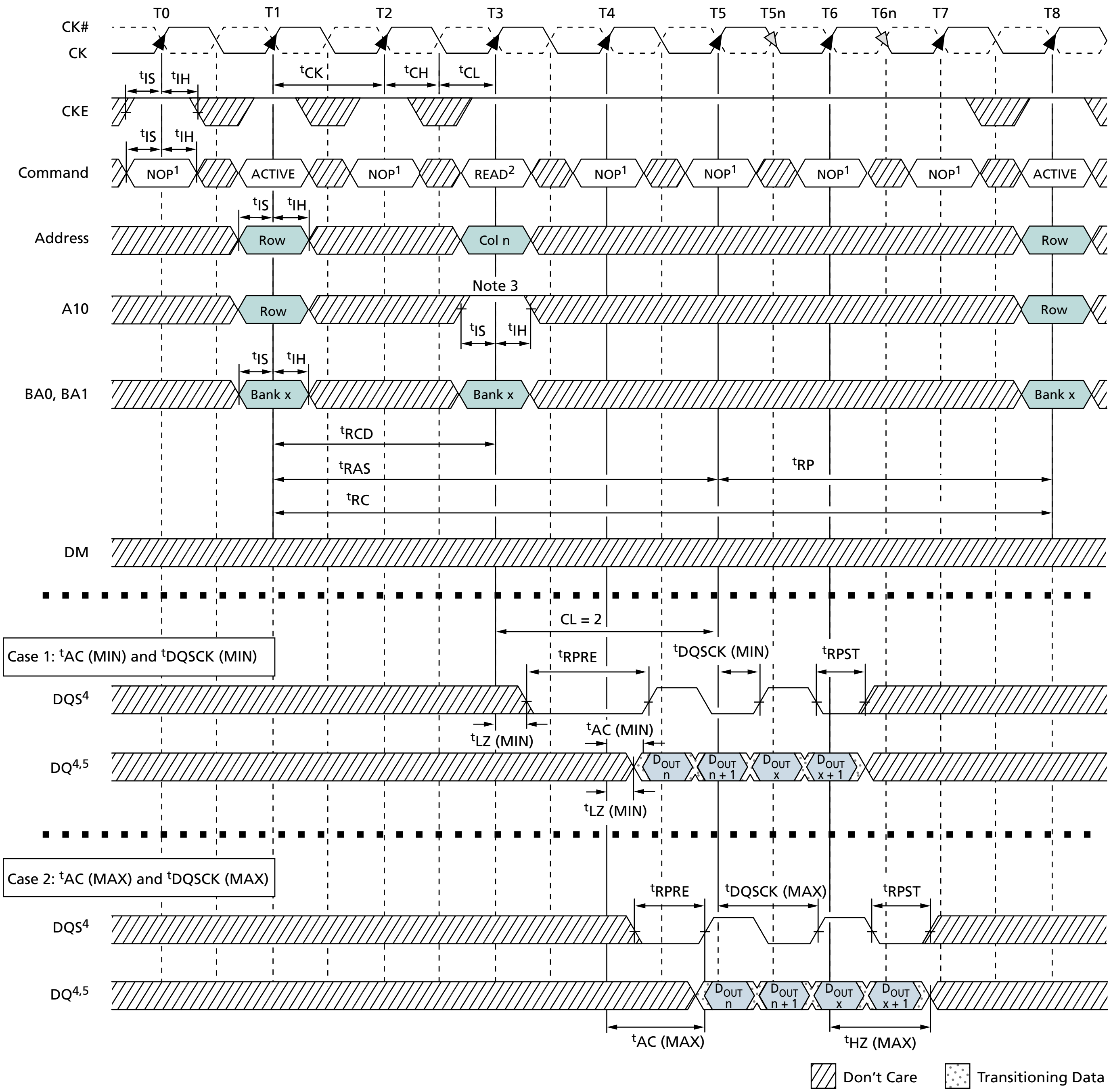
This device supports ^tRAS lock-out. In the case of a single READ with auto precharge or single WRITE with auto precharge issued at ^tRCD (MIN), the internal precharge will be delayed until ^tRAS (MIN) has been satisfied.

Bank READ operations with and without auto precharge are shown in Figure 50 (page 90) and Figure 51 (page 91). Bank WRITE operations with and without auto precharge are shown in Figure 52 (page 92) and Figure 53 (page 93).

Concurrent Auto Precharge

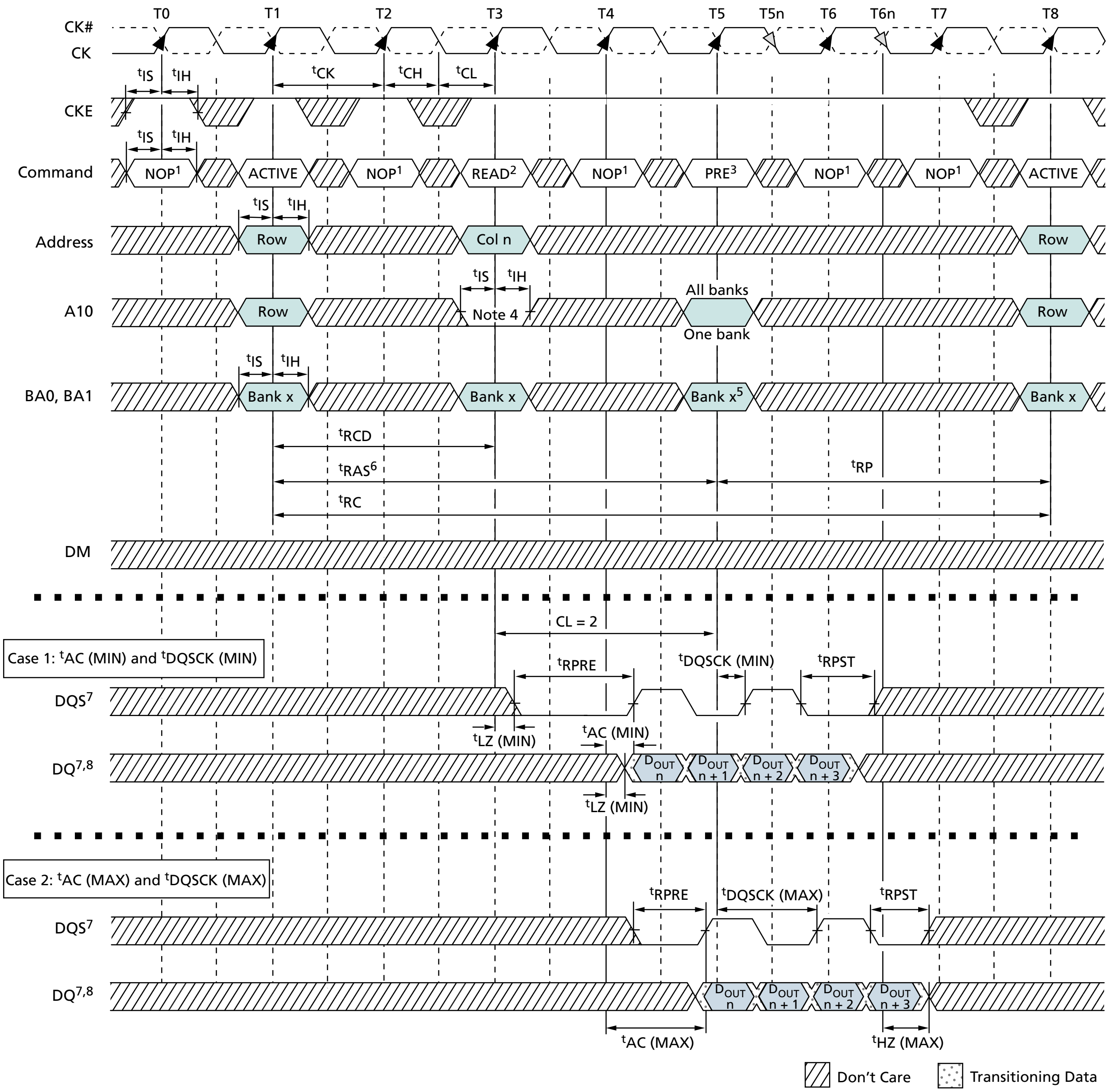
This device supports concurrent auto precharge such that when a READ with auto precharge is enabled or a WRITE with auto precharge is enabled, any command to another bank is supported, as long as that command does not interrupt the read or write data transfer already in process. This feature enables the precharge to complete in the bank in which the READ or WRITE with auto precharge was executed, without requiring an explicit PRECHARGE command, thus freeing the command bus for operations in other banks.

Figure 50: Bank Read – With Auto Precharge



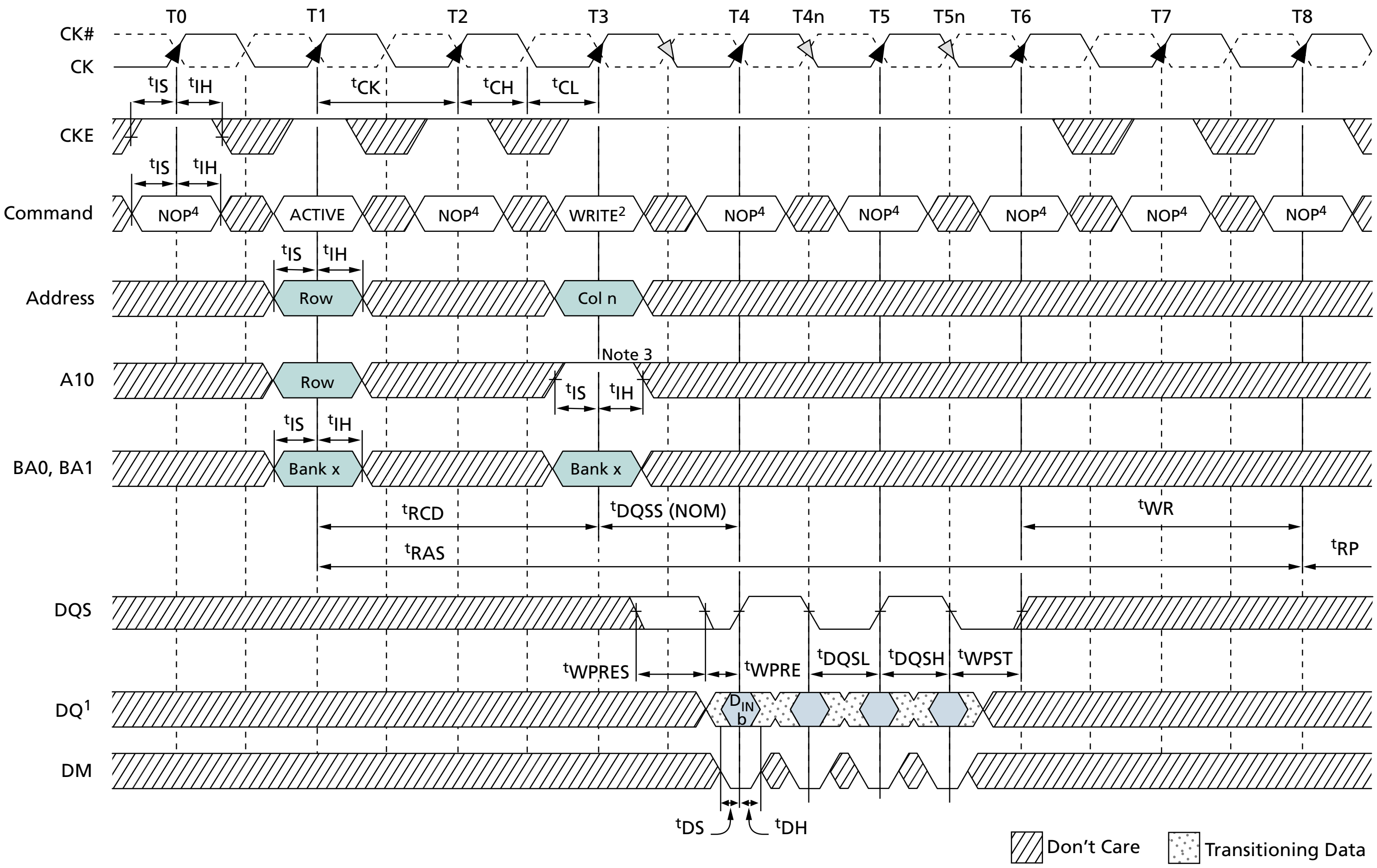
Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4 in the case shown.
3. Enable auto precharge.
4. Refer to Figure 35 (page 73) and Figure 36 (page 74) for detailed DQS and DQ timing.
5. D_{OUT} *n* = data-out from column *n*.

Figure 51: Bank Read – Without Auto Precharge



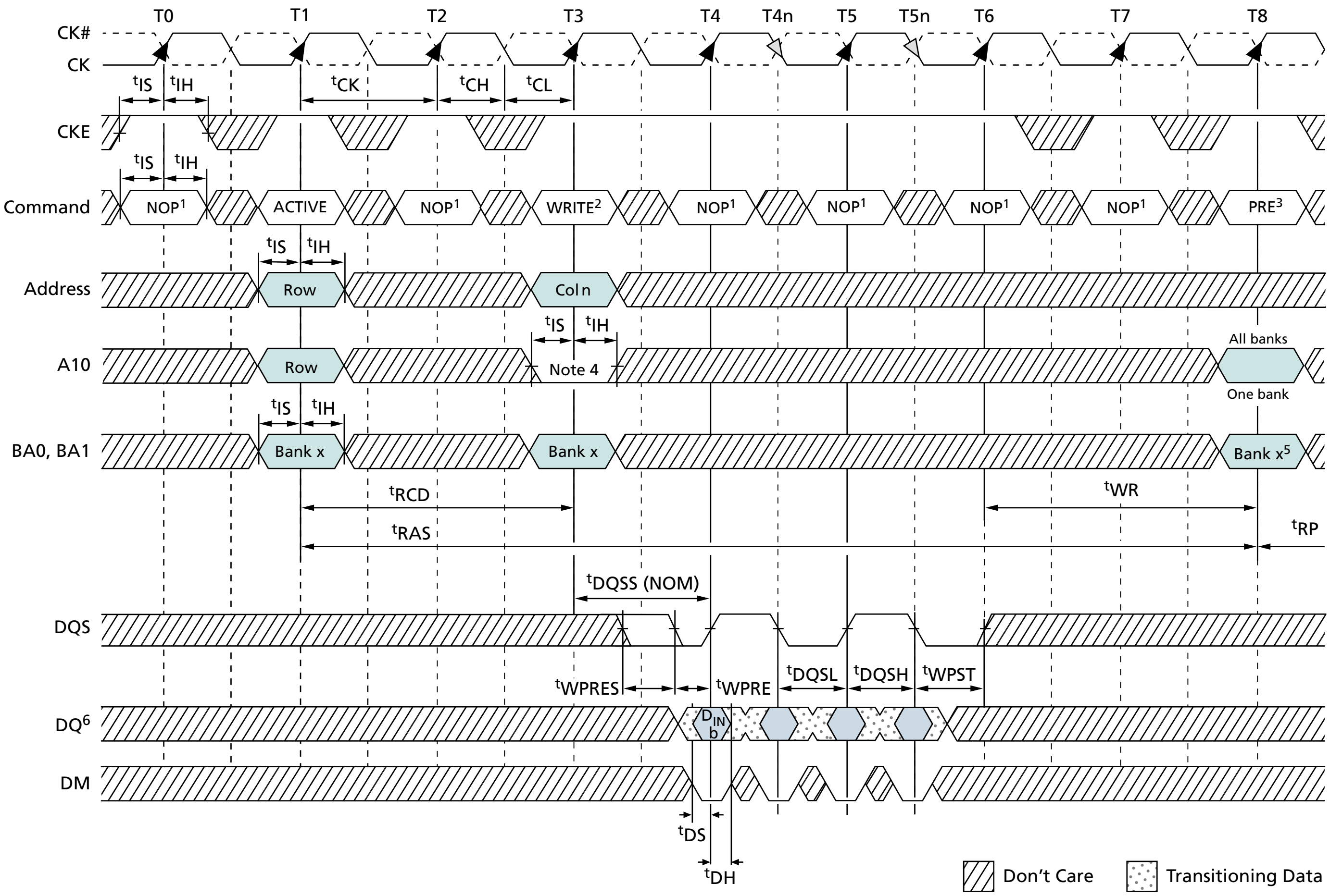
Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4 in the case shown.
3. PRE = PRECHARGE.
4. Disable auto precharge.
5. Bank *x* at T5 is "Don't Care" if A10 is HIGH at T5.
6. The PRECHARGE command can only be applied at T5 if tRAS (MIN) is met.
7. Refer to Figure 35 (page 73) and Figure 36 (page 74) for DQS and DQ timing details.
8. D_{OUT} *n* = data out from column *n.*

Figure 52: Bank Write – With Auto Precharge



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4 in the case shown.
3. Enable auto precharge.
4. D_{IN} *n* = data-out from column *n*.

Figure 53: Bank Write – Without Auto Precharge



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4 in the case shown.
3. PRE = PRECHARGE.
4. Disable auto precharge.
5. Bank x at T8 is "Don't Care" if A10 is HIGH at T8.
6. D_{OUT} *n* = data-out from column *n*.

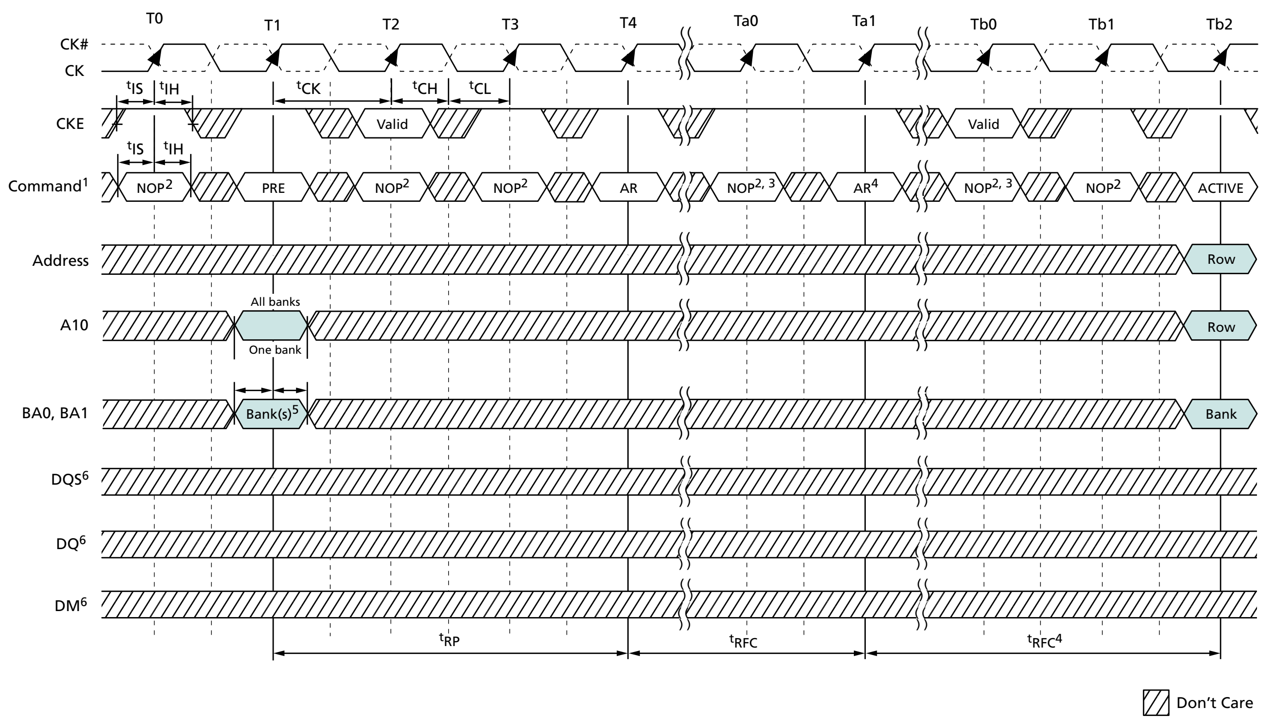
AUTO REFRESH Operation

Auto refresh mode is used during normal operation of the device and is analogous to CAS#-BEFORE-RAS# (CBR) REFRESH in FPM/EDO DRAM. The AUTO REFRESH command is nonpersistent and must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits a “Don’t Care” during an AUTO REFRESH command.

For improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. The auto refresh period begins when the AUTO REFRESH command is registered and ends ^tRFC later.

Figure 54: Auto Refresh Mode



Notes:
1. PRE = PRECHARGE; AR = AUTO REFRESH.
2. NOP commands are shown for ease of illustration; other commands may be valid during this time. CKE must be active during clock positive transitions.
3. NOP or COMMAND INHIBIT are the only commands supported until after ^tRFC time; CKE must be active during clock positive transitions.
4. The second AUTO REFRESH is not required and is only shown as an example of two back-to-back AUTO REFRESH commands.
5. Bank *x* at T1 is “Don’t Care” if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (for example, must precharge all active banks).
6. DM, DQ, and DQS signals are all “Don’t Care”/High-Z for operations shown.

Although it is not a JEDEC requirement, CKE must be active (HIGH) during the auto refresh period to provide support for future functional features. The auto refresh period begins when the AUTO REFRESH command is registered and ends ^tRFC later.

SELF REFRESH Operation

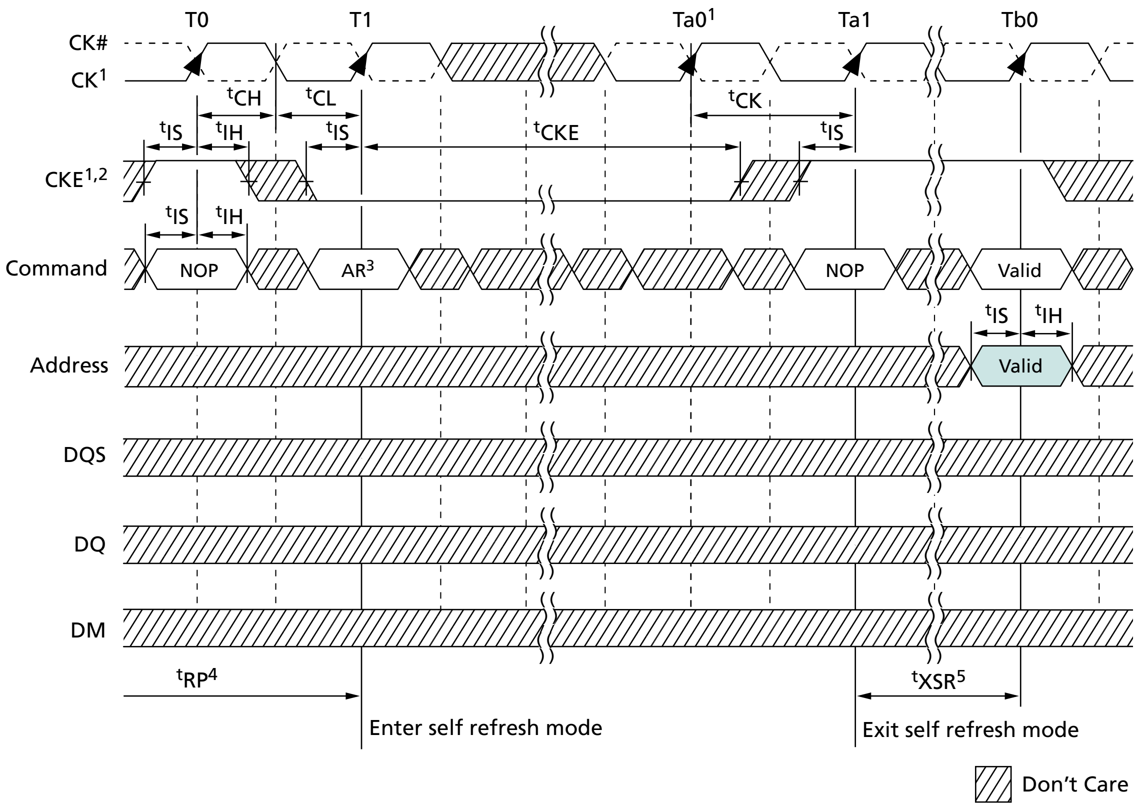
The SELF REFRESH command can be used to retain data in the device while the rest of the system is powered down. When in self refresh mode, the device retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command, except that CKE is disabled (LOW). All command and address input signals except CKE are "Don't Care" during self refresh.

During self refresh, the device is refreshed as defined in the extended mode register. (see Partial-Array Self Refresh (page 61).) An internal temperature sensor adjusts the refresh rate to optimize device power consumption while ensuring data integrity. (See Temperature-Compensated Self Refresh (page 60).)

The procedure for exiting self refresh requires a sequence of commands. First, CK must be stable prior to CKE going HIGH. When CKE is HIGH, the device must have NOP commands issued for ^{t}XSR to complete any internal refresh already in progress.

During SELF REFRESH operation, refresh intervals are scheduled internally and may vary. These refresh intervals may differ from the specified ^{t}REFI time. For this reason, the SELF REFRESH command must not be used as a substitute for the AUTO REFRESH command.

Figure 55: Self Refresh Mode



Notes:
1. Clock must be stable, cycling within specifications by Ta0, before exiting self refresh mode.
2. CKE must remain LOW to remain in self refresh.
3. AR = AUTO REFRESH.
4. Device must be in the all banks idle state prior to entering self refresh mode.
5. Either a NOP or DESELECT command is required for ^tXSR time with at least two clock pulses.

Power-Down

Power-down is entered when CKE is registered LOW. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates all input and output buffers, including CK and CK# and excluding CKE. Exiting power-down requires the device to be at the same voltage as when it entered power-down and received a stable clock. Note that the power-down duration is limited by the refresh requirements of the device.

When in power-down, CKE LOW must be maintained at the inputs of the device, while all other input signals are "Don't Care." The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command). NOP or DESELECT commands must be maintained on the command bus until ^{t}XP is satisfied. See Figure 57 for a detailed illustration of power-down mode.

Figure 56: Power-Down Entry (in Active or Precharge Mode)

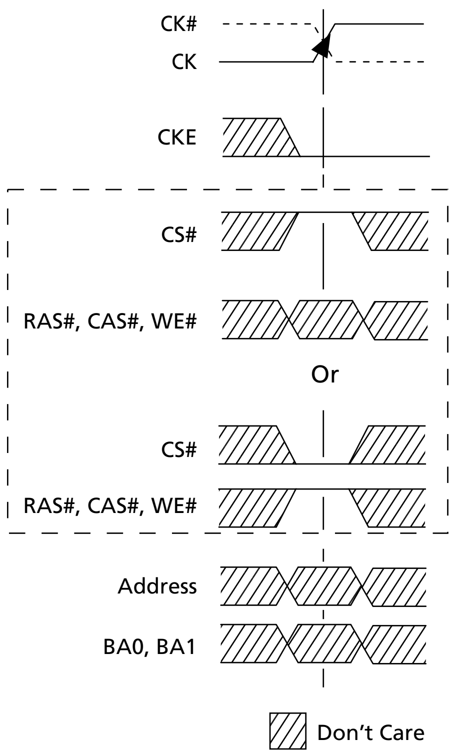
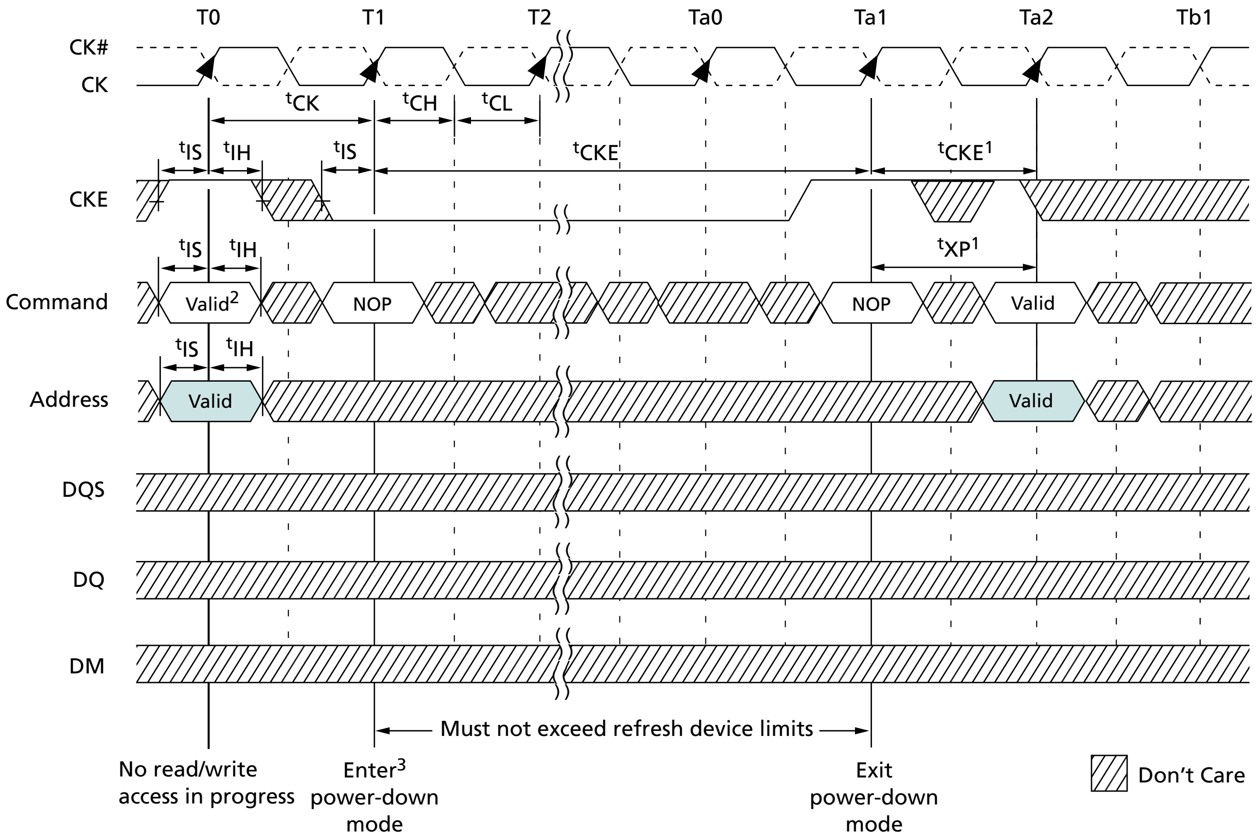


Figure 57: Power-Down Mode (Active or Precharge)



Notes: 1. ^tCKE applies if CKE goes LOW at Ta2 (entering power-down); ^tXP applies if CKE remains HIGH at Ta2 (exit power-down).

2. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down. If this command is an ACTIVE (or if at least 1 row is already active), then the power-down mode shown is active power-down.

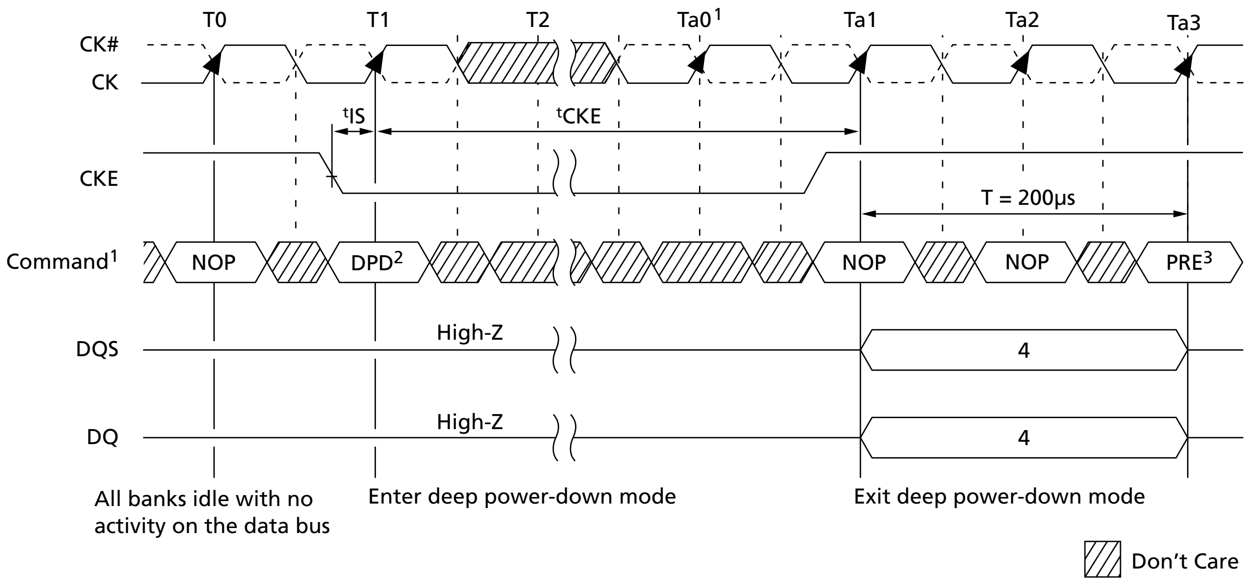
3. No column accesses can be in progress when power-down is entered.

Deep Power-Down

Deep power-down (DPD) is an operating mode used to achieve maximum power reduction by eliminating power to the memory array. Data will not be retained after the device enters DPD mode.

Before entering DPD mode the device must be in the all banks idle state with no activity on the data bus (^tRP time must be met). DPD mode is entered by holding CS# and WE# LOW with RAS# and CAS# HIGH at the rising edge of the clock while CKE is LOW. CKE must be held LOW to maintain DPD mode. The clock must be stable prior to exiting DPD mode. To exit DPD mode, assert CKE HIGH with either a NOP or DESELECT command present on the command bus. After exiting DPD mode, a full DRAM initialization sequence is required.

Figure 58: Deep Power-Down Mode



Notes:
1. Clock must be stable prior to CKE going HIGH.
2. DPD = deep power-down.
3. Upon exit of deep power-down mode, a full DRAM initialization sequence is required.
4. DQ and DQS bus may not be High-Z during this period. Packages or applications that share the data bus are not allowed to have other activity on the data bus for 200µs after the deep power-down exit.

Clock Change Frequency

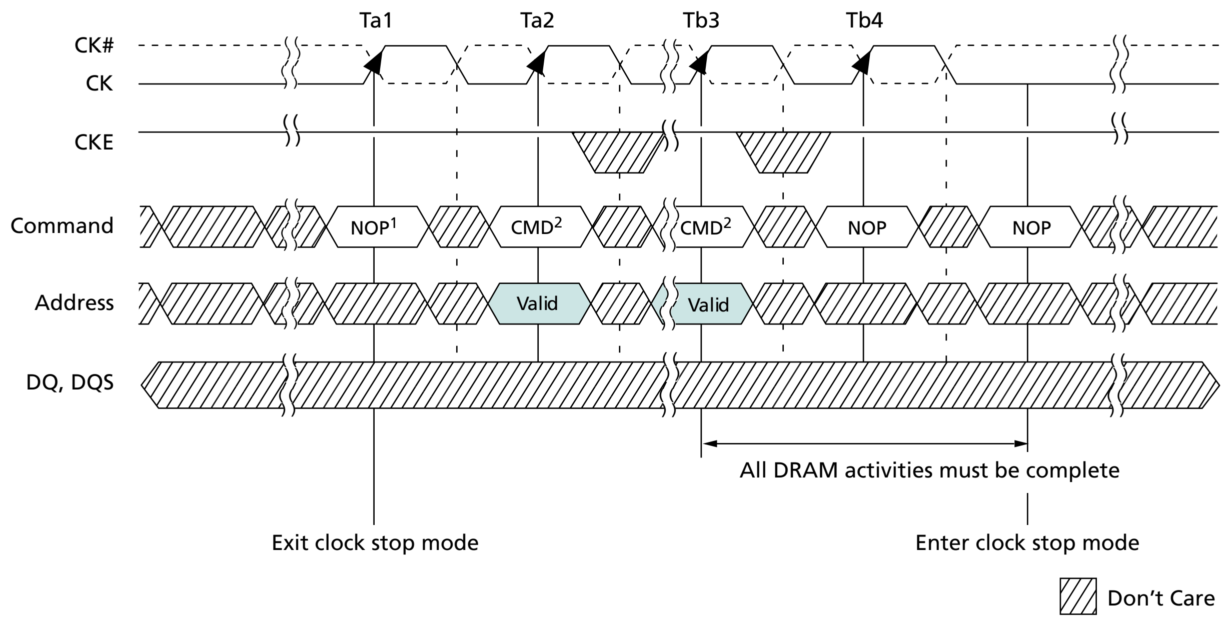
One method of controlling the power efficiency in applications is to throttle the clock that controls the device. The clock can be controlled by changing the clock frequency or stopping the clock.

The device enables the clock to change frequency during operation only if all timing parameters are met and all refresh requirements are satisfied.

The clock can be stopped altogether if there are no DRAM operations in progress that would be affected by this change. Any DRAM operation already in process must be completed before entering clock stop mode; this includes the following timings: ^tRCD, ^tRP, ^tRFC, ^tMRD, ^tWR, and ^tRPST. In addition, any READ or WRITE burst in progress must be complete. (See READ Operation and WRITE Operation.)

CKE must be held HIGH with CK = LOW and CK# = HIGH for the full duration of the clock stop mode. One clock cycle and at least one NOP or DESELECT is required after the clock is restarted before a valid command can be issued.

Figure 59: Clock Stop Mode



Notes: 1. Prior to Ta1, the device is in clock stop mode. To exit, at least one NOP is required before issuing any valid command.
2. Any valid command is supported; device is not in clock suspend mode.

Revision History

Rev. F - 9/14

- Replaced KK package with KQ package
- 11/14 - corrected package typo from VFBGA to WFBGA on KQ package

Rev. E – 7/14

- Updated I_{DD0}, I_{DD4R}, and I_{DD4W} for WT and IT grades

Rev. D – 3/14

- Added special options
- Updated part numbering chart

Rev. C – 2/14

- Updated Deep Power-Down Mode figure and added Note 4

Rev. B – 1/14

- Corrected BQ and DD dimensions in Figure 1

Rev. B – 11/13

- Replaced B7, CX, JV, KQ, MA, and MC packages with BQ, DD, KK, and SA packages codes
- Added -48 speed grade
- To Production

Rev. A – 07/13

- Initial release; Reference document: 2Gb x16, x32 Automotive Mobile LPDDR SDRAM data sheet; Doc Version: t79m_ait_aat_mobile_lpddr.pdf - Rev. A 08/12 EN; PDF: 09005aef84e25f2e; Preliminary status

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-4000
www.micron.com/products/support Sales inquiries: 800-932-4992

This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.