

USB PD Controller Series

Stand-Alone PD Controller for Sink BD93E11GWL EVK

BD93E11GWL-EVK-001 (Stand-Alone)

Introduction

The User's Guide describes the series of required procedures to operate and evaluate the EVK of the PD controller BD93E11GWL for Sink. The document also contains the circuit components, the operating procedures, and the Application Data.

Overview

BD93E11GWL-EVK-001 implements Stand-Alone PD Controller IC of BD93E11GWL in Sink mode. This EVK performs the Type-C connection and make PD contracts with the attached Source device according to the configuration of the DIP switches on the board. The EVK assumes Stand-Alone operation in the Dead Battery mode, so this EVK does not need an external power source and works as a VBUS powered product. The board will supply power and voltage via VSNK terminal based on the negotiation contracted with the source. Therefore, any existing board that is powered by an AC adapter or a regulated power supply up to 80W/20V can work and be evaluated with the EVK as a Type-C/PD power source.

EVK Operation Condition

Parameter	Min	Typ	Max	Units	Conditions
VBUS Power Supply	3.67	5.0	22	V	
VSRC5V Power Supply	3.1	5.0	5.5	V	
VSNK Output Voltage	4.75	5.0	22	V	Guaranteed by USB Standard and connected Source.
VSNK Output Current Range			3.0/5.0	A	Depending on the Type-C cable. The actual load current is depending on the sink device operation that connects to VSNK terminal.

EVK Overview

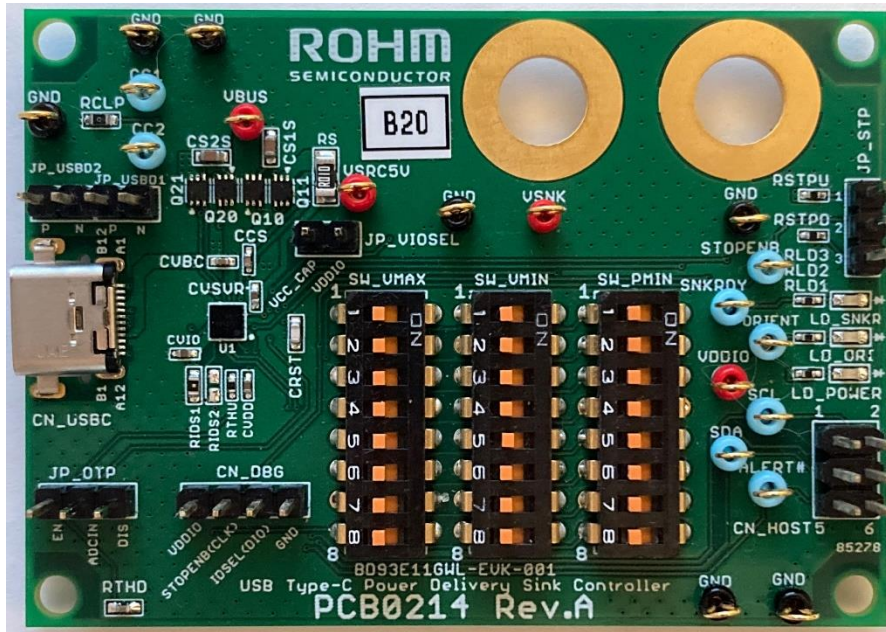


Figure 1. BD93E11GWL-EVK-001(Top View)

Descriptions of EVK function

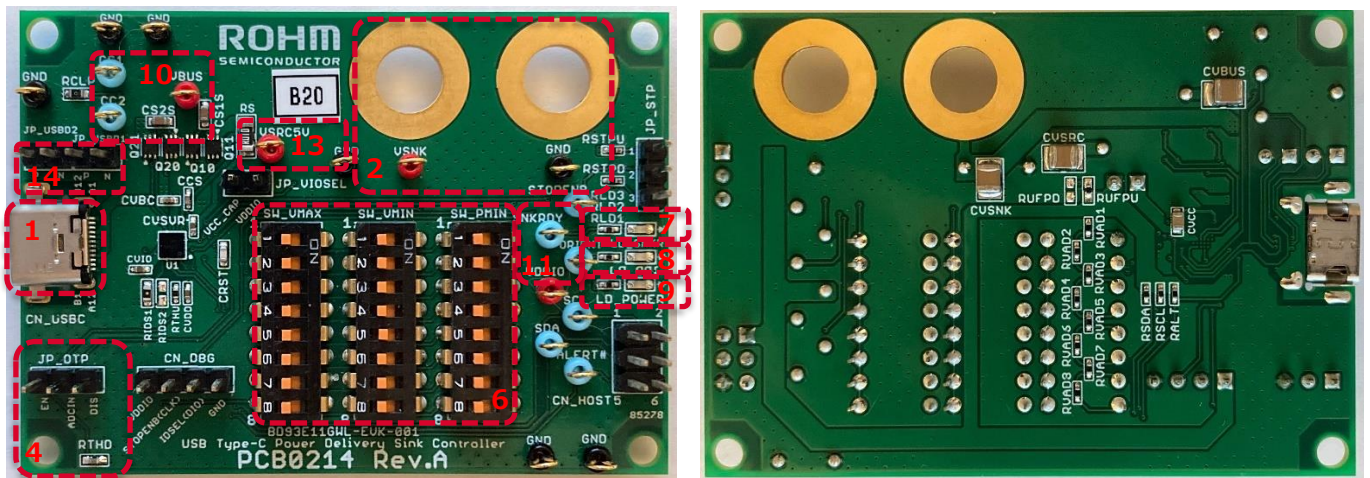


Figure 2. The descriptions of the part of BD93E11GWL-EVK-001

This EVK has the functions that are defined in Table 1. Other than the functions listed, this EVK User Guide does not support it.

Table 1. The descriptions of the available functions

No.	Function	Silk Indication	Description	Default Setting
1	Type-C Receptacle	CN_USB	Certified USB Type-C Receptacle TID: 5,200,000,020	-
2	Input System Power/Ground	VSNK, GND	The output for a system / an existing external board.	-
4	Enable OTP	JP_OTP	Enable/Disable configuration for (OTP) Over Temperature Protection with the PTC thermistor. EN short: Enabled / EN Open: Disabled	Enabled
6	Select Auto Sink Request	SW_VMAX, SW_VMIN, SW_PMIN	Automatically selects the range of Power and Voltage to be contracted by USB PD.	VMAX = Set8, VMIN = Set1, PMIN = Set1, (5V to 20V, 0.5W)
7	LED of Sink Ready	LD_SNKR	Indicates when a series of process including the Type-C connection and USB PD contract is completed. Note that the indication doesn't mean that VBUS is supplying VSNK. The LED also turns on when the 5V PD contract is established due to the less power capability of the source side.	-
8	LED of ORIENT	LD_ORI	Indicates the orientation (Normal or Flip) of the connected Type-C, ON: Connected by CC2 OFF: Connected by CC1 or disconnected.	-
9	LED of POWER	LD_POWER	Indicates the condition of the LSI. ON: The power is supplied to the LSI. OFF: No power supply.	-
10	Monitor USB PD Communication	CC1, CC2,	Monitor terminals for Type-C voltage level and USB PD Communication.	-
	Monitor VBUS condition	VBUS	Monitor terminal for VBUS voltage.	-
11	Monitor Functions	SNKRDY, ORIENT,	Monitor terminal for LSI features.	-
13	SRC Power of 5V	VSRC5V	5V power supply from external power source. Connect VSRC5V to a 5V supply that is normally derived from the system battery.	-
14	USB 1.x / 2.0 communication	JP_USBD1, JP_USBD2	Communication terminal for USB 1.x / 2.0 D+(P)/D-(N) JP_USBD1: CC1 side JP_USBD2: CC2 side	-

We cannot respond to inquiries other than the functions above.

EVK schematic

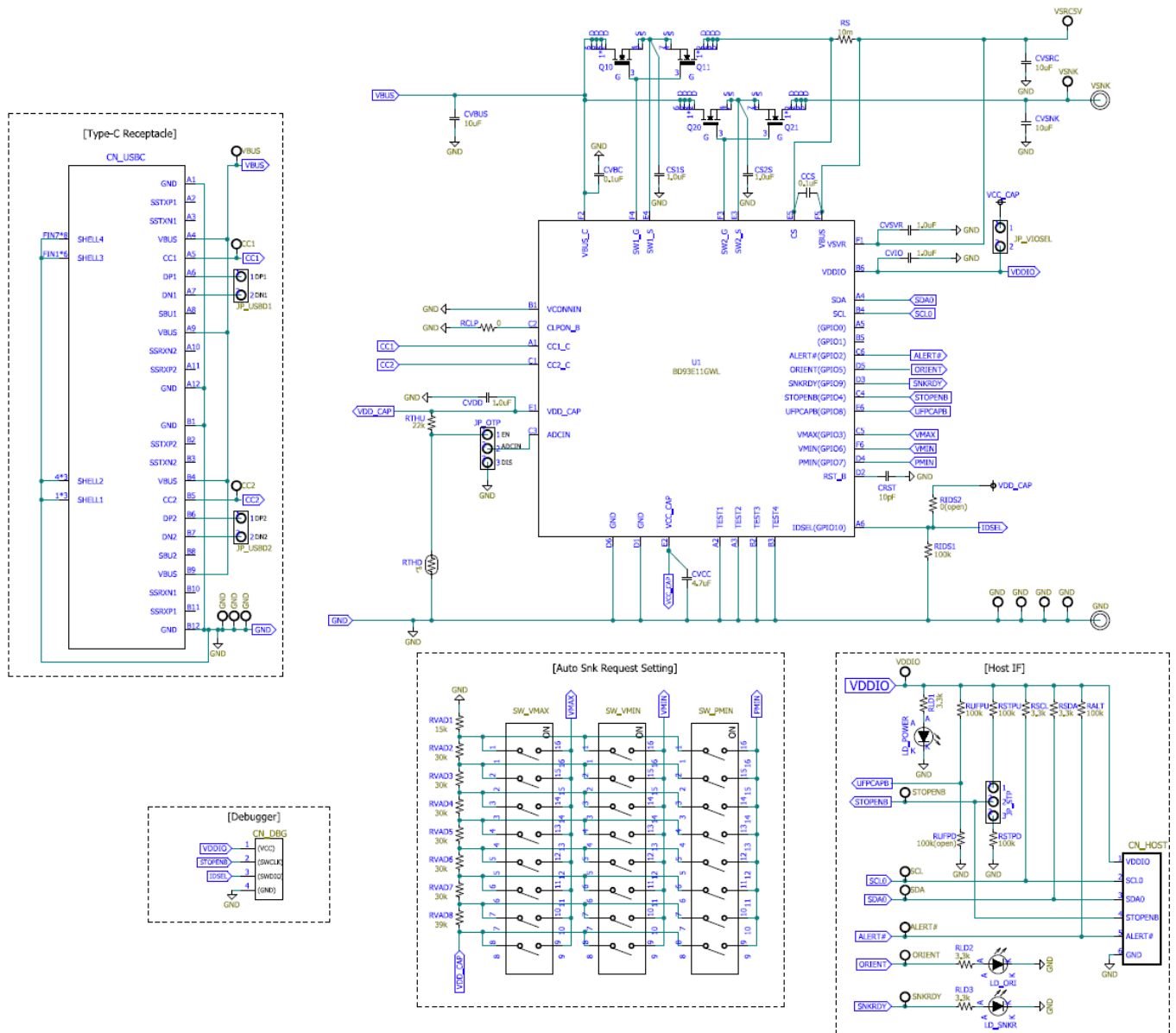


Figure 3. BD93E11GWL-EVK-001 Schematic

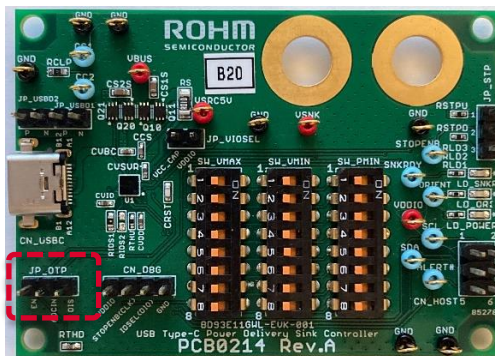
Operating Sequence

(The preparation for power up)

1. Confirm if both JP_VIOSEL and JP_STP are shorted by a jumper pin. The EVK cannot work correctly if there are no jumper pins on these terminals. It is highly recommended to be checked (These jumpers are present by default.).



2. Short EN and ADCIN on JP_TOP if the Over Temperature Protection with the external PTC thermistor is in use. If not in use, short ADCIN and SGND.



3. Set SW_VMAX, SW_VMIN and SW_PMIN according to required PD contract. Please refer to Figure 9 for further information.



4. When connecting the existing system board for evaluation, connect the EVK into the existing system board before power up as shown in Figure 6.

(Check operation)

1. Prepare any source device, e.g., Type-C/PD adapter, then connect to the Type-C receptacle on the EVK via a cable. Please insert a USB Type-C/PD protocol analyzer between the Source device and EVK if it is required to monitor the transaction on CC signals as shown in Figure 8.
2. When LD_VBRDY lights up, it shows that the connection with a Source device is completed. LD_ORI shows the orientation of the inserted plug.
3. Confirm the contracted voltage from VSNK using a digital multimeter as shown in Figure 4.

If there is no monitored VSNK voltage, below are the possible reasons:

- Type-C devices cannot be identified by the port as Sink or Source device. It is possible that the connected device is a Sink device.
- The connected Source device cannot meet the required power or voltage configured by PMIN or VMIN.
- There may be a latched-off state that is caused by the overvoltage on the Source or the EVK side due to the inrush current by the load connected on VSNK. The EVK has no countermeasures for inrush current so it is required for a system to prevent it.

Please check both Figure 16 and Figure 17 to conform the correct behavior of the Type-C/PD connection.

(Connection examples and details)

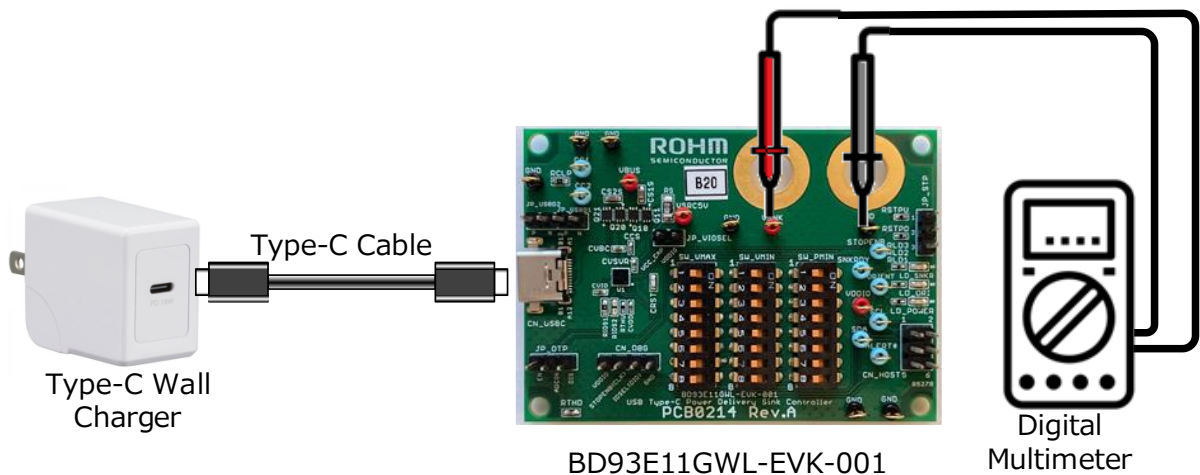


Figure 4. An evaluation for only EVK with Type-C cable

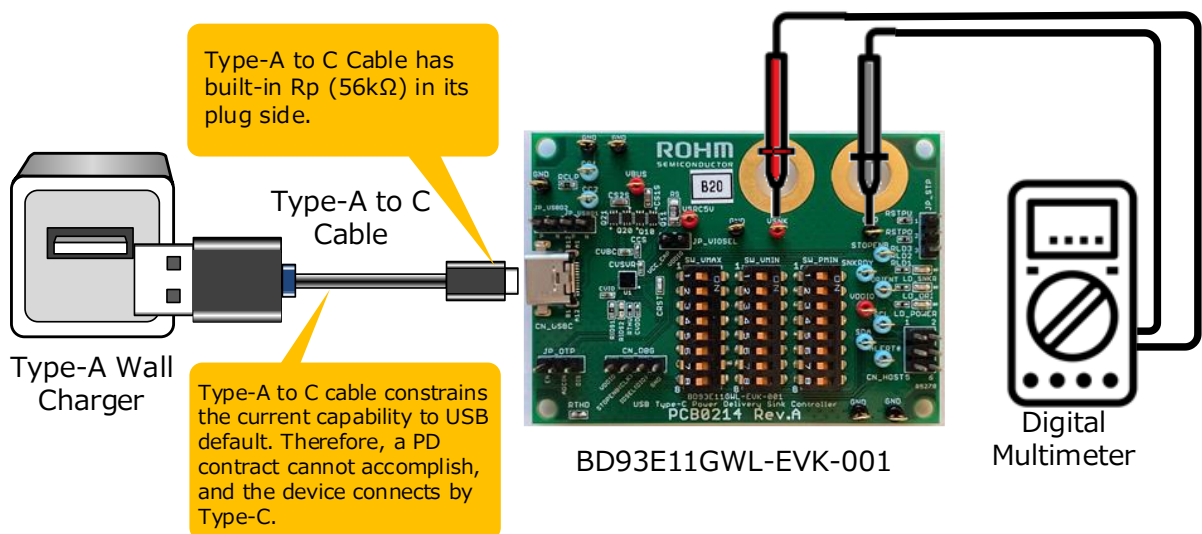


Figure 5. An example of the connection with Type-A to C Cable

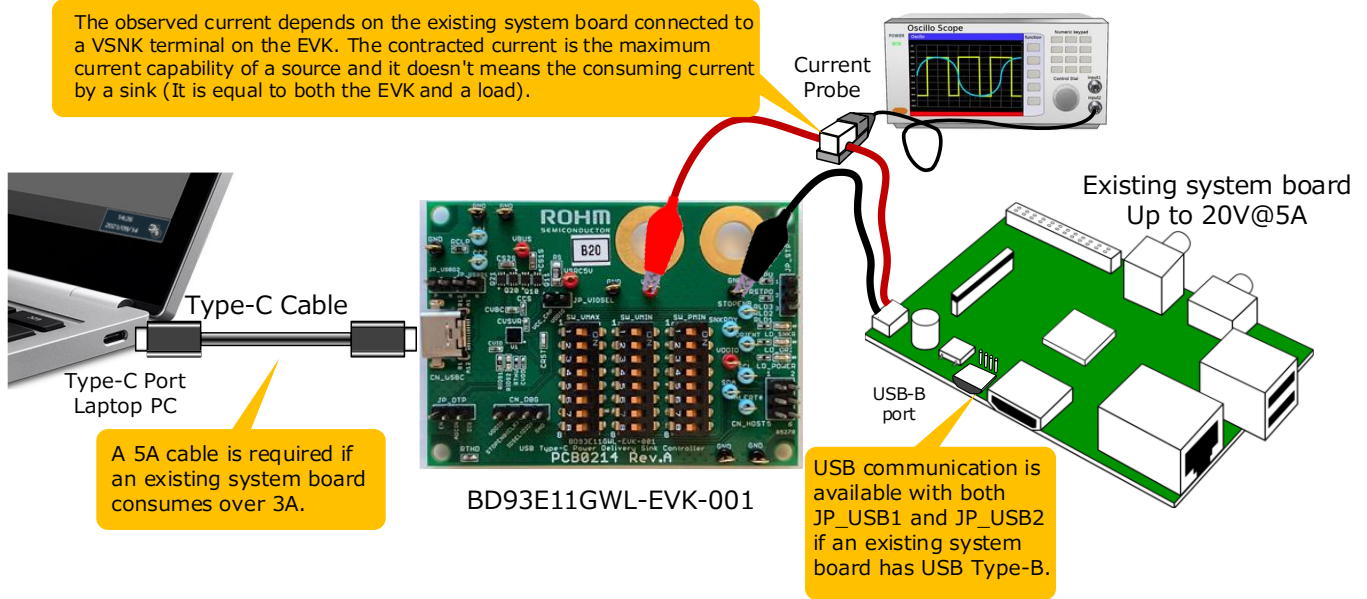


Figure 6. An example of the connection of the EVK supplying power to an existing system board

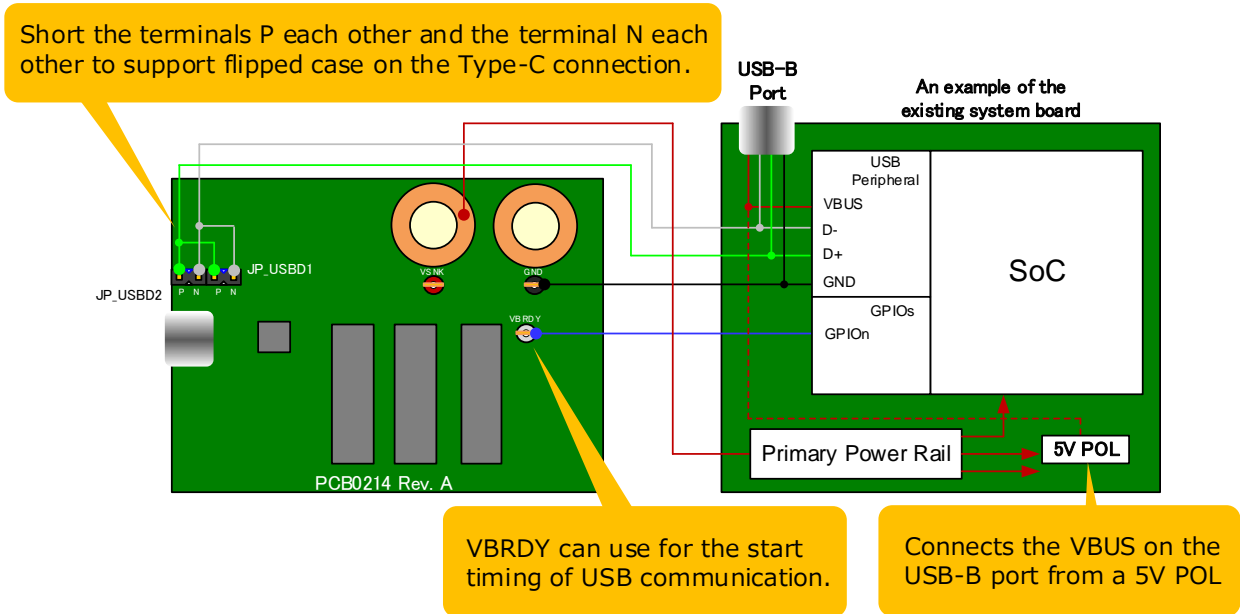


Figure 7. An example of USB connection on an existing system board

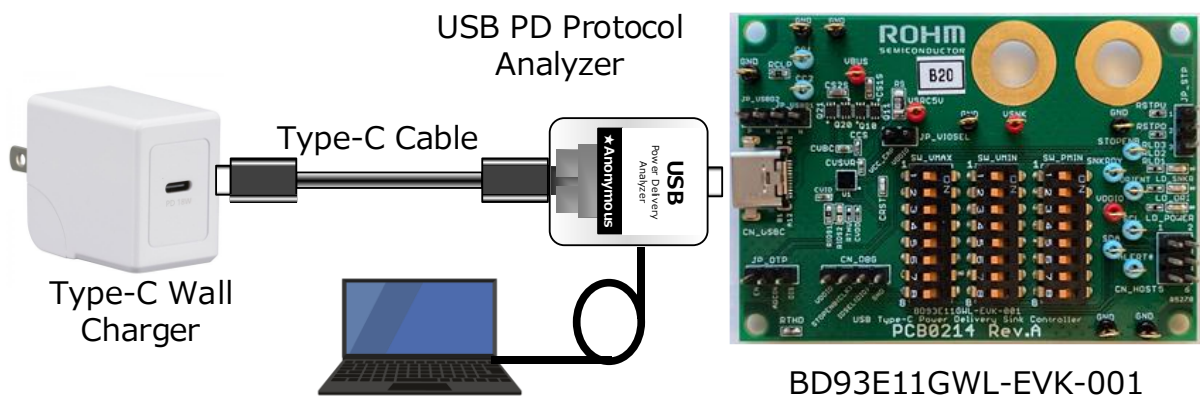


Figure 8. An example of the connection with a protocol analyzer for PD communication

(Change configuration of the PD contracts)

Note: The configurations of SW_VMAX, SW_VMIN, and SW_PMIN are stored upon power up. [Dynamically changing the DIP switches will not change the configuration during operation.](#) Please do the following procedures to set the new configuration. Settings will be reflected after a power cycle of the EVK.

1. Turn off VSRC5V if powered up.
2. Unplug the Type-C cable from the Type-C Receptacle and disconnect it from the Source device.
3. Change SW_VMAX, SW_VMIN, and SW_PMIN according to the requirement.
4. Power up VSRC5V if necessary. The new configuration is stored at power up.
5. Reconnect the Source device to the Type-C receptacle of the EVK via the Type-C cable.

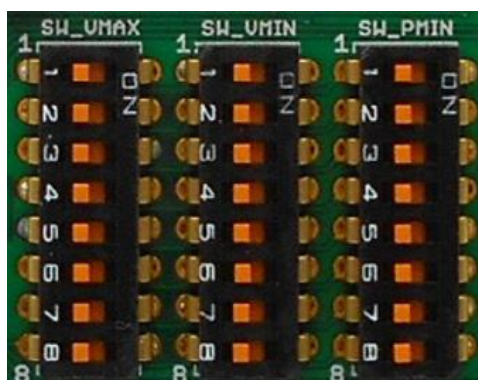
Configuring the USB PD contract range

This EVK can set the range of USB PD contract automatically according to SW_VMAX, SW_VMIN, SW_PMIN DIP switch settings. The EVK can make a contract with a PD source that has a range within the "USB PD Contractable Range" shown in Figure 9. The EVK requires a power cycle to update the range assigned by SW_VMAX, SW_VMIN, and SW_PMIN. A power cycle occurs by both disconnecting from a Source device and losing power from VSRC5V. If there is no VSRC5V, only disconnecting from a Source device is required.

A USB PD contract is determined by USB PD communication on either CC1 or CC2 between a Source and a Sink device after the Type-C connection. Please refer to Figure 17 regarding USB PD communication waveform.

Note: Each DIP switch must only have one position at ON. Multiple positions are not allowed, as it does not guarantee the expected operation.

Table 2. The table for the range of PD contract by SW_VMAX / SW_VMIN / SW_PMIN



Set	SW_VMAX[V]	SW_VMIN[V]	SW_PMIN[W]
1	5*	5*	0.5
2	9*	9*	7.5
3	12	12	15
4	15*	15*	27
5	16	16	36
6	18	18	45
7	19	19	60
8	20*	20*	80

* Required voltage depending on the power specified for the Source device specified in the PDP Rating in the USB PD standard. Others are optional.

Table 3. The detailed information for three DIP switches

Terminal	SW_VMAX	SW_VMIN	SW_PMIN
Description	<ul style="list-style-type: none"> The upper limit voltage for the USB PD contract. The device does not make a contract that exceeds this value. The value should not be less than SW_VMIN. It will operate as 5V@0.1A if SW_VMAX is less than SW_VMIN. 	<ul style="list-style-type: none"> The lower limit voltage for the USB PD contract. The device does not make a contact that falls under this value. Set SW_VMAX equal to SW_VMIN if a specific fixed voltage is required. The value should not be more than SW_VMAX. It will operate as 5V@0.1A if SW_VMIN is more than SW_VMAX. 	<ul style="list-style-type: none"> The lower limit power for the USB PD contract and it shall meet the minimum power that can operate the sink device. The product cannot make a contract with the Source device if the power capability is not enough. The maximum current for the sink on the contracted current is up to the maximum current capability of a source. If a setting where SW_PMIN / min (SW_VMAX or SW_VMIN), exceeds 5A, then It will operate as 5V@0.1A.

Figure 9 shows the specific range by SW_VMAX, SW_VMIN, and SW_PMIN that allows USB PD Contract.

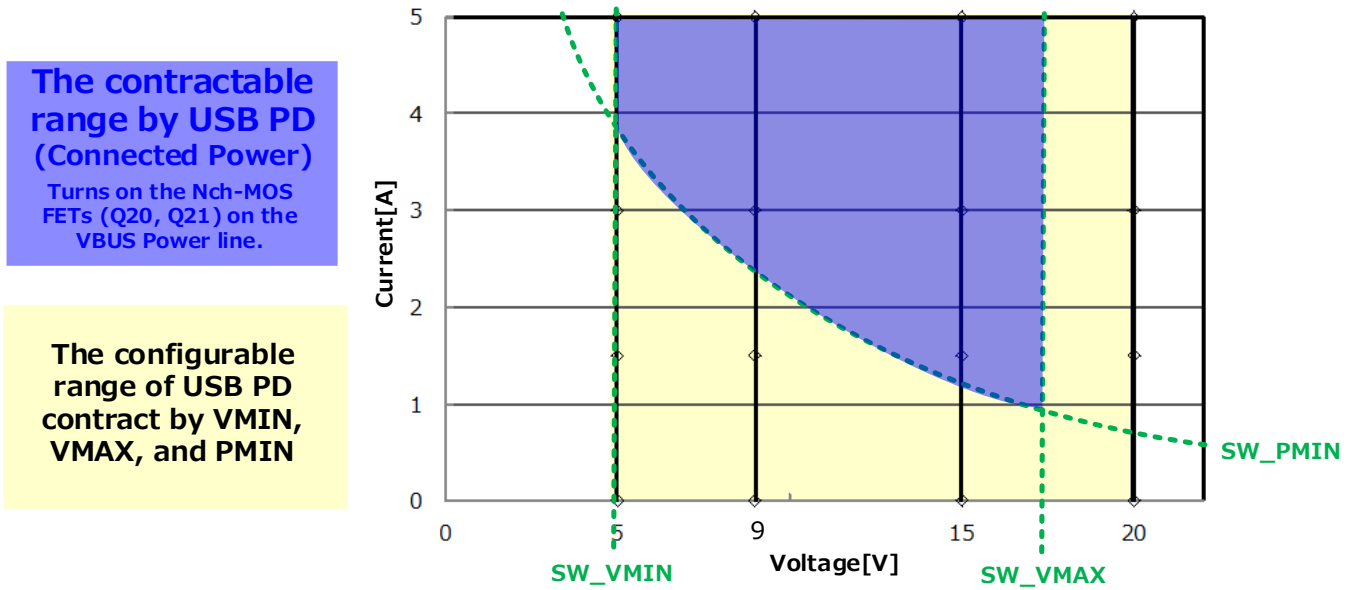


Figure 9. USB PD Contractable Range

Figure 10 shows the contracted power data objects (PDO) with a 45W source supporting 5V, 9V and 15V when DIP switches are set to SW_VMAX = 15V (Set to 4), SW_VMIN = 9V (Set to 3), and SW_PMIN = 15W (Set to 3).

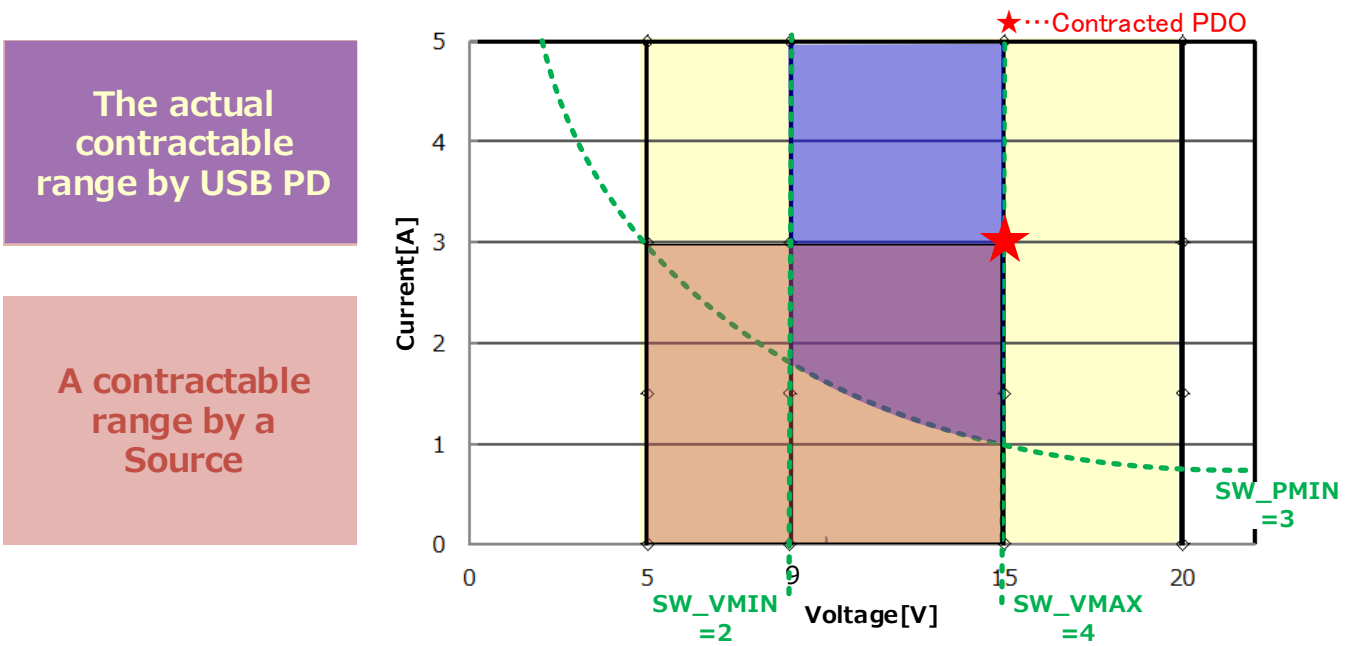


Figure 10. The contractable range with a source under the example

According to the ★ sign, the contracted PDO is specified to the maximum power within the USB PD contractable range. USB PD standard mandates the specific voltages according to the power of the contracted Source. 5V, 9V, 15V, and 20V are mandatory and other voltage are optional.

For example, if the EVK that SW_VMAX is set to 12V and connected to the Source device specified in Figure 10 where the Source device does not have 12V as an option, then the contract with the EVK will be PDO of 9V@3A.

Over temperature protection by an external PTC thermistor

This EVK has the over temperature protection using thermistor RTHD mounted on the board. The detection threshold of the protection is set to 120°C and when the temperature around the PTC thermistor reaches the set temperature, the device turns off the Nch-MOS FET (Q20 and Q21) on VBUS power line to isolate VBUS from the system safely. To enable this protection, connect JP_OTP EN and ADSIN with a jumper pin.

Other than the temperature detected at RTHU, the over temperature protection can be triggered by the specific applied voltage as defined in Table 4.

Table 4. The parameters of the OTP with PTC thermistor

Items	
Detection temperature [°C]	120
Implemented PTC thermistor as RTHU	MURATA PRF15BD102QB6RC
ON Threshold [V]	0.780
OFF Threshold [V]	0.470
Divided resistance RTHU [Ω]	22k

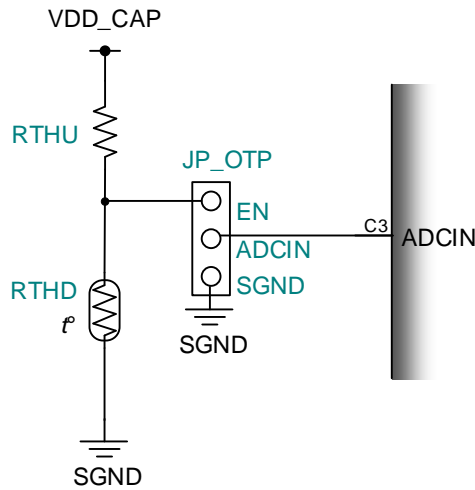


Figure 11. OTP Schematic Circuit

Parts List

Table 5. Parts list

Part	Value	Manufacturer	Model Number	Size [mm(inch)]
IC				
U1	BD93E series	ROHM	BD93E11GWL	2.63x2.63
FET				
Q10, Q11, Q20, Q21	RW4E075AJ	ROHM	RW4E075AJ	HEML1616L7
Capacitor				
CCS	0.1 μ F	TDK	CGA2B3X7R1H104K050BB	1005(0402)
CRST	10pF	AVX	06035A100FAT2A	1608(0603)
CS1S, CS2S	1 μ F	TDK	CGA3E3X5R1H105K080AB	1608(0603)
CVDD	1 μ F	TDK	CGA2A1X5R1C105K033BC	1005(0402)
CVBC	0.1 μ F	TDK	CGA2B3X7R1H104K050BB	1005(0402)
CVBUS, CVSRC, CVSINK	10 μ F	MURATA	GCM32EC71H106KA03	3225(1210)
CVCC	4.7 μ F	MURATA	GRM188R61E475KE11	1608(0603)
CVIO, CVSVR	1 μ F	TDK	CGA2A1X5R1C105K033BC	1005(0402)
CVS	0.1 μ F	TDK	CGA2B3X7R1H104K050BB	1005(0402)
Resistor				
RS	10m Ω	STACKPOLE	CSRF1206FT10L0	3216(1206)
RIDS1	100K Ω	ROHM	ESR03EZPF1003	1608(0603)
RIDS2	0 Ω	Not Mount	-	1608(0603)
RALT, RSTPU, RSTPD	100K Ω	ROHM	MCR01MZPF1003	1005(0402)
RUFPU	100K Ω	ROHM	MCR01MZPF1003	1005(0402)
RUFPD	100K Ω	Not Mount	-	1608(0603)
RLD1, RLD2, RLD3, RSCL, RSDA	3.3k Ω	ROHM	MCR01MZPF3301	1005(0402)
RTHU	22K Ω	ROHM	MCR01MZPF2202	1005(0402)
RVAD1	15K Ω	VISHAY DALE	CRCW040215K0FKED	1005(0402)
RVAD2, RVAD3, RVAD4, RVAD5, RVAD6, RVAD7	30K Ω	ROHM	MCR01MZPF3002	1005(0402)
RVAD8	39K Ω	ROHM	MCR01MZPF3902	1005(0402)
RCLP	0 Ω	ROHM	MCR03EZPJ000	1608(0603)
RTHD	PRF15BD102QB6RC	MURATA	PRF15BD102QB6RC	1608(0603)
Connector				
CN_USBC	DX07B024JJ1R1500	JAE	DX07B024JJ1R1500	Type-C Receptacle
LED				
LD_POWER	LED	ROHM	SML-D12M8WT86	LED
LD_ORI	LED	ROHM	SML-D12M8WT86	LED
LD_SNKR	LED	ROHM	SML-D12M8WT86	LED
Switch				
SW_VMAX, SW_VMIN, SW_PMIN	DipSW "Totsu" 8 poles	OMRON	"Kata" A6T-8104	DIP8_SW
Contact Pin				
TP1, TP2	CC1	MAC 8	LC-2-G-White	TESTPIN
TP3, TP4, TP5, TP6	VBUS	MAC 8	LC-2-G-Red	TESTPIN
TP7, TP8, TP9, TP10, TP11, TP12	SCL	MAC 8	LC-2-G-White	TESTPIN
TPGND1, TPGND2, TPGND3	SGND	MAC 8	LC-2-G-Black	TESTPIN
TPGND4 TPGND5 TPGND6 TPGND7	GND	MAC 8	LC-2-G-Black	TESTPIN
TERMINAL	VSNK	Not Mount	-	TESTPIN
TERMINAL	GND	Not Mount	-	TESTPIN

Part	Value	Manufacturer	Model Number	Size [mm(inch)]
CN_HOST	HDR2X3	ADAM TECH	PH2-06-UA	HDR2X3
CN_DBG	HDR1X4	ADAM TECH	PH1-04-UA	HDR1X4
JP_STP, JP_OTP	HDR1X3	ADAM TECH	PH1-03-UA	HDR1X3
JP_VIOSEL JP_USBD1 JP_USBD2	HDR1X2	ADAM TECH	PH1-02-UA	HDR1X2

Board Layout

EVK PCB Information

Number of Layers	Material	Board Size	Copper Thickness
4	FR-4	70mm x 50mm x 1.6mm	1oz (35µm)

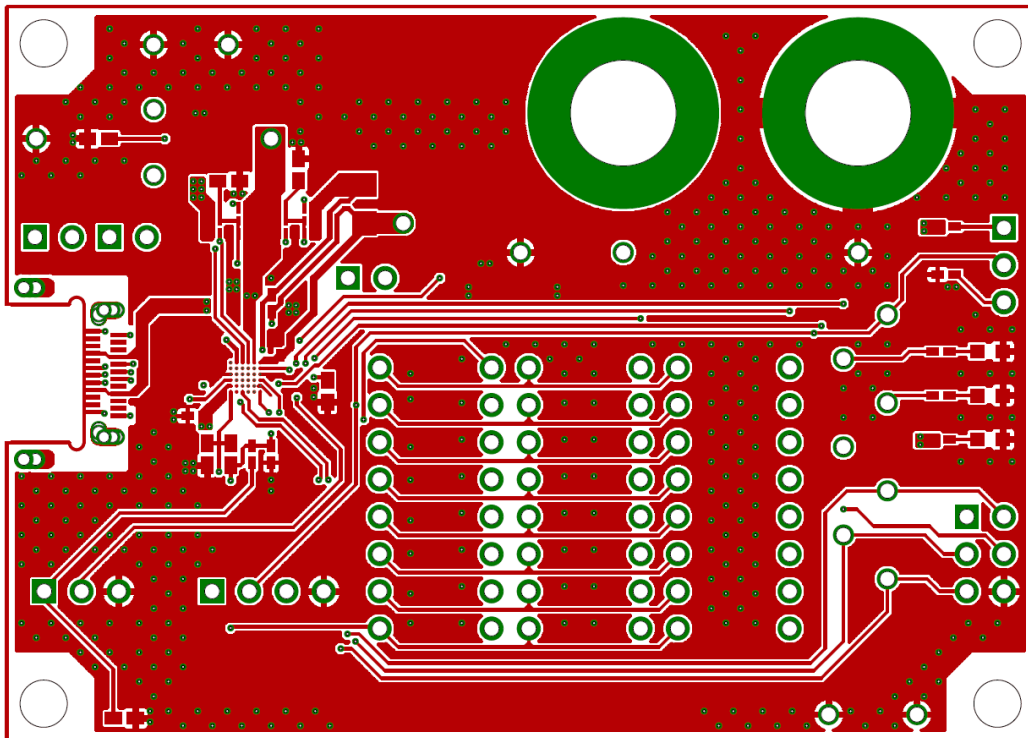


Figure 12. Top Layer (Top View)

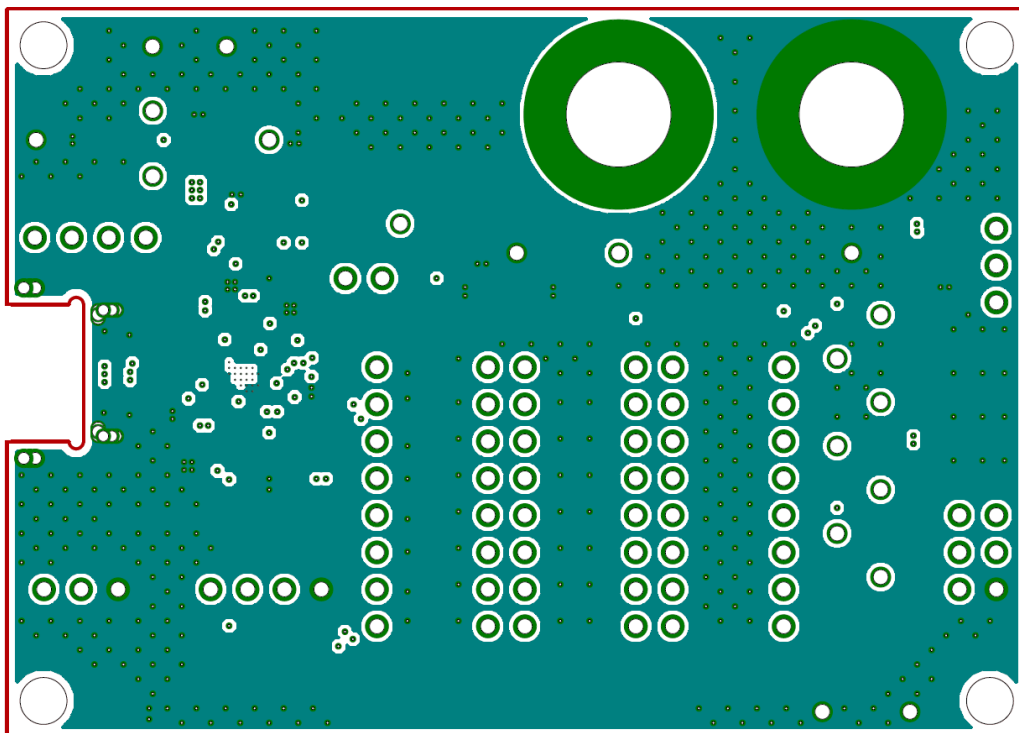


Figure 13. Middle Layer 1 (Top View)

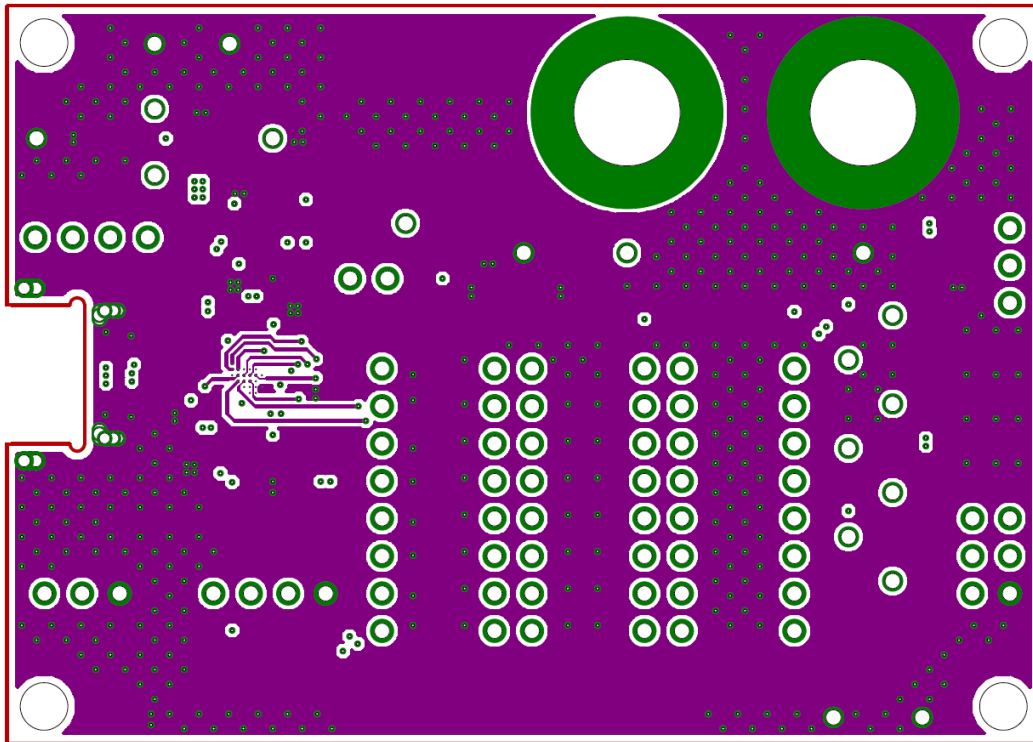


Figure 14. Middle Layer 2 (Top View)

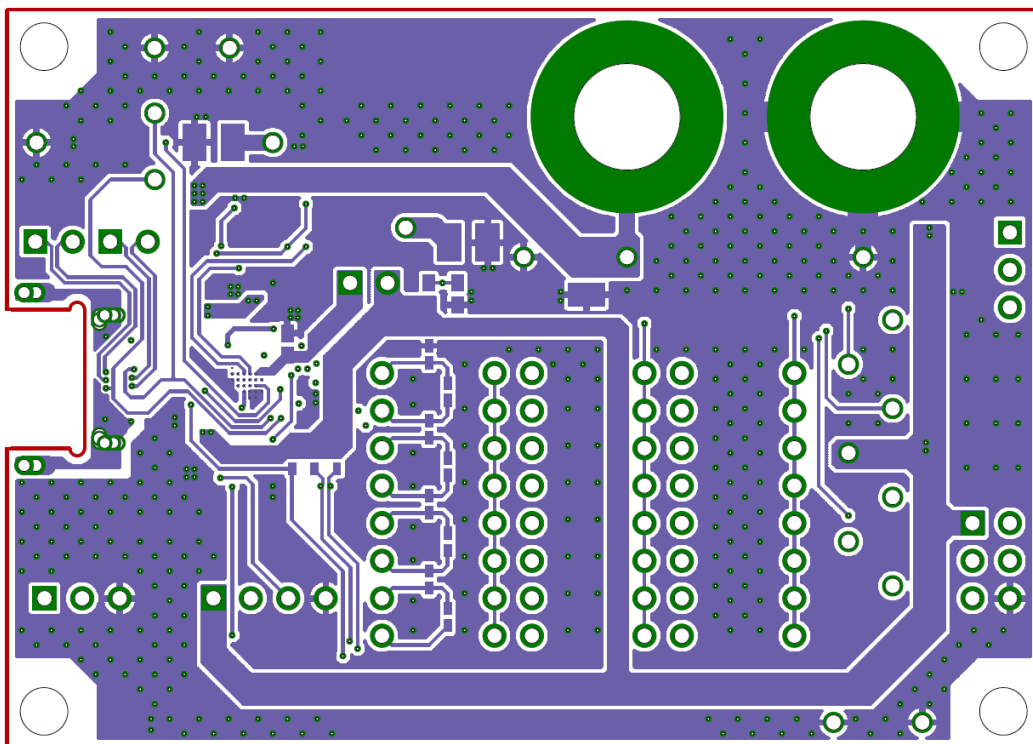


Figure 15. Bottom Layer (Top View)

Reference Application Data

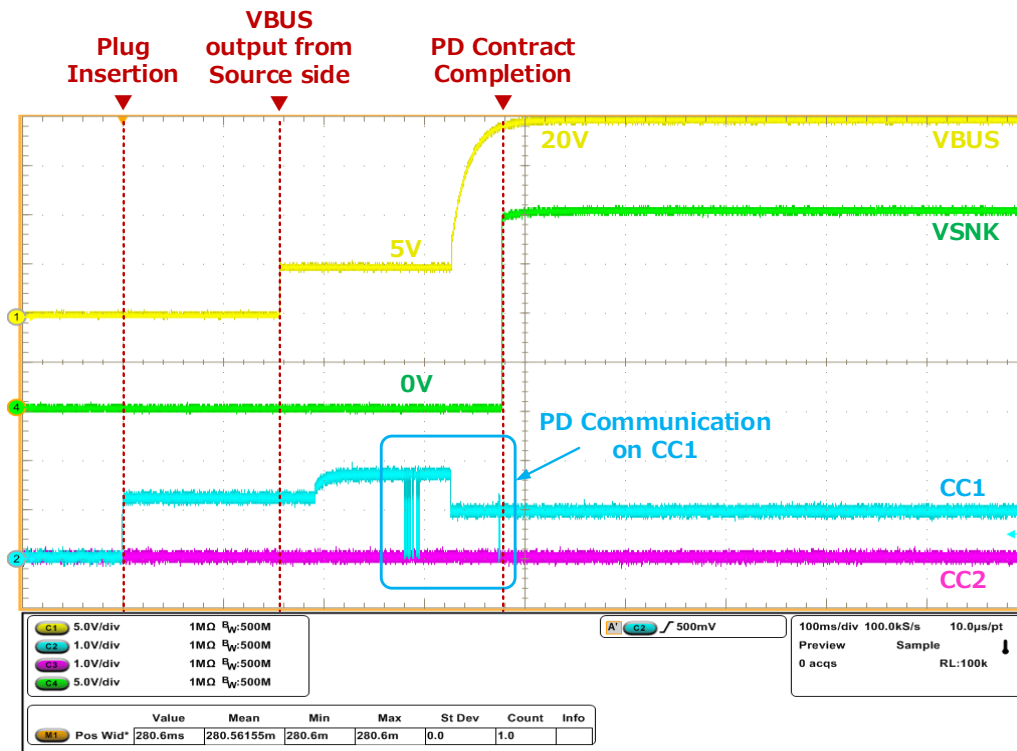


Figure 16. The waveform of the USB PD Negotiation at 20V

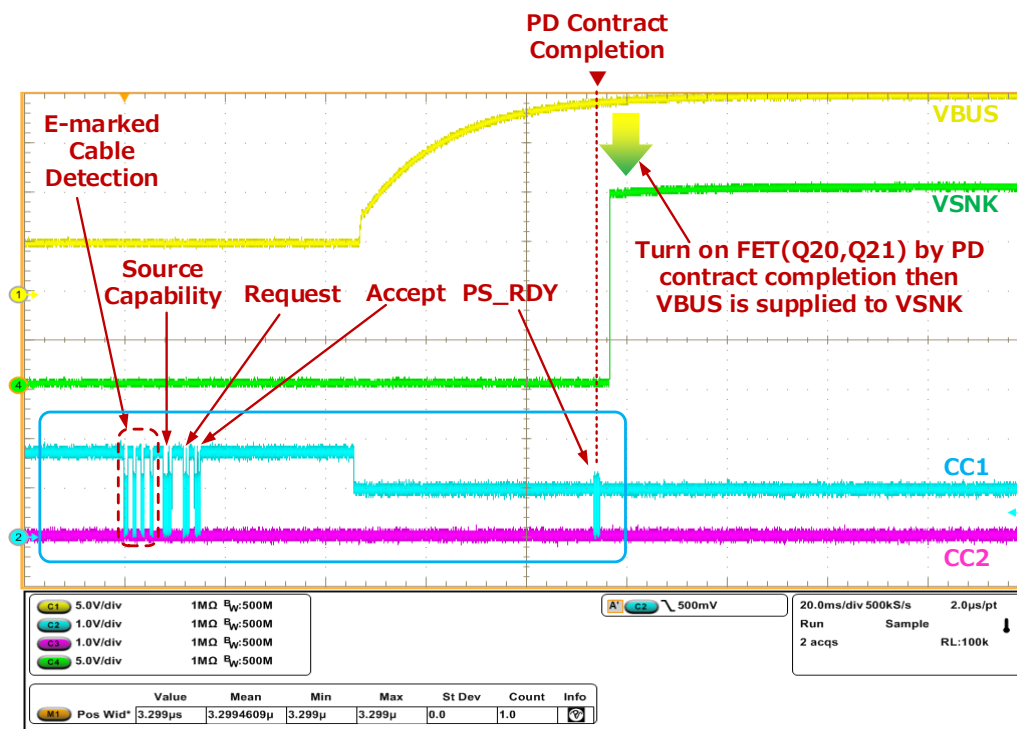


Figure 17. The Waveform of the USB PD Negotiation at 20V (Detailed PD Communication)

The USB PD communication on CC1 or CC2 signal results in BMC modulated digital communication with 1 UI of 300kHz. It is necessary to check this communication for analyzing and debugging when introducing the USB PD system. Below are some relatively inexpensive protocol analyzers that have enough merits in the USB IF workshop.

- Total Phase USB Power Delivery Analyzer TP350110
- TELEDYNE LECROY Mercury T2C Protocol Analyzer USB-TMPD-M02-X

Revision History

Date	Revision Number	Description
Oct. 19. 2021	001	Initial release

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