SY6340

150mA LDO Regulator

General Description

The SY6340 is a 150mA precise LDO. The device provides programmable output voltage with +/-2% accuracy. The ultra low drop out voltage, wide input voltage range and low ground current make it suitable for USB and portable electronics applications with different inputs. Other features include the operation stability with low ESR ceramic capacitors due to the internal compensation, logic enable control, thermal shutdown, current limit, reverse leakage current protection.

The SY6340 is available in SOT23-5/DFN2×2-6 package.

Ordering Information

SY6340 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6340AAC	SOT23-5	----
SY6340DEC	DFN2×2-6	

Features

- Wide input voltage range: 2.3V to 30V
- Low dropout voltage(300mV @ 150mA)
- Low ground current
- Ultra low shutdown current
- High output accuracy of +/-2% over operating temperature range
- Stable with small ceramic capacitors
- Excellent load and line regulation
- 150mA output current capability
- Output current limitation
- Reverse leakage current protection
- Reverse input voltage protection
- TTL logic enable input
- Thermal shutdown
- RoHS Compliant and Halogen Free
- Compact SOT23-5/ DFN2×2-6 package

Applications

- Battery powered applications
- Consumer and portable products
- Notebook
- Smart phones
- SMPS post-regulator/ DC-DC modules

Typical Applications

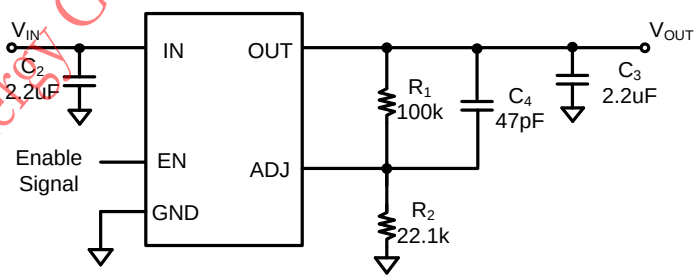


Figure 1. Schematic Diagram

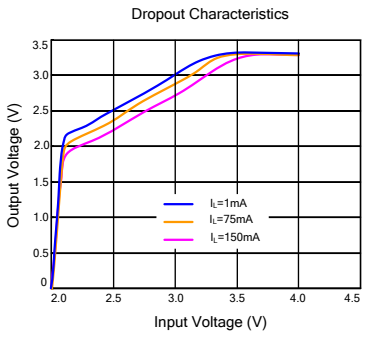
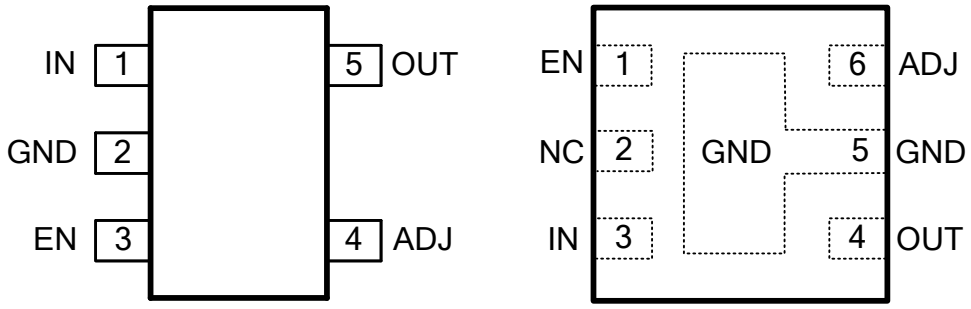


Figure 2. Dropout Characteristics

Pinout (top view)



(SOT23-5) (DFN2×2-6)

Top mark: **JN*xyz*** for SY6340AAC(Device code: JN, ***x=year code, y=week code, z= lot number code***)
Top mark: **PE*xyz*** for SY6340DEC(Device code: PE, ***x=year code, y=week code, z= lot number code***)

Pin Name	SOT23-5	DFN2×2-6	Pin Description
IN	1	3	Supply input pin.
GND	2	5	Ground pin.
OUT	5	4	LDO output pin.
EN	3	1	Enable pin. Pull it low to shutdown or pull it high to enable, do not leave open.
ADJ	4	6	Output voltage adjust pin. Feedback the output voltage through resistor voltage divider network. $V_O = 0.6 \times (1 + \frac{R1}{R2})$

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -20V to 36V
Output Voltage ---------- 0.3V+VIN
EN Voltage ---------- -0.3V to 0.3V+VIN
ADJ Voltage ---------- 0V to 3.6V
Power Dissipation, P_D @ T_A = 25°C SOT23-5/ DFN2×2-6 ---------- 0.6/0.7W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 100/62°C/W
θ_{JC} ---------- 25/8.5°C/W
Junction Temperature Range ---------- 125°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.3V to 30V
Output Voltage ---------- 0.3V+V_{IN}
EN Voltage ---------- 0V to 0.3V+V_{IN}
Junction Temperature (T_J) ---------- -40°C to +125°C

Electrical Characteristics

(V_{IN} =V_{OUT}+1V, or V_{IN}=2.3V, V_{EN}=V_{IN},TA = 25°C unless otherwise specified)

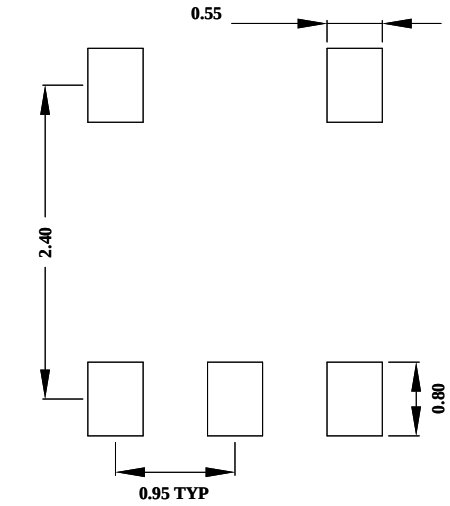
Parameter	Symbol	Test Conditions	Min	Typical	Max	Unit
Input Voltage	V_{IN}		2.3		30	V
Output Voltage accuracy	V_{OUT}	I_O=100uA	-2		2	%
Line Regulation	ΔV_{LNR}	V_{IN}=(V_{OUT}+0.3) to 30V, I_O=100uA		0.04		%
Load Regulation	ΔV_{LDR}	I_O=0.1mA to 150mA		0.25	1	%
Dropout Voltage	V_{IN}-V_{OUT}	I_O=10mA		20		mV
		I_O=50mA		100		mV
		I_O=100mA		200		mV
		I_O=150mA		300		mV
Shutdown Current	I_{SHDN}	V_{EN}=0V, V_{IN}=24V		1		μA
Quiescent Current	I_Q	I_O=0.1mA		18	30	μA
		I_O=150mA		450		μA
Current limit	I_{LIM}	V_{OUT}=0.9×V_{OUT}(normal)		350	500	mA
Reverse leakage current limit	I_{RLK}	V_{IN}=-15V, Load=500ohms		-0.1		uA
Power-supply Rejection Ratio	PSRR	f=1kHz, C_{OUT}=10uF		50		dB
Input UVLO Threshold	V_{UVLO}	V_{IN} rising			2.25	V
UVLO Hysteresis	V_{UVLO_th}			100		mV
Shutdown discharge Resistor				500		Ω
Enable Input logic-High Voltage	V_{EN_H}	V_{IN}=2.8 to 5.5V	1.5			V
Enable Input logic-Low Voltage	V_{EN_L}	V_{IN}=2.8 to 5.5V			0.6	V
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown hysteresis	T_{HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

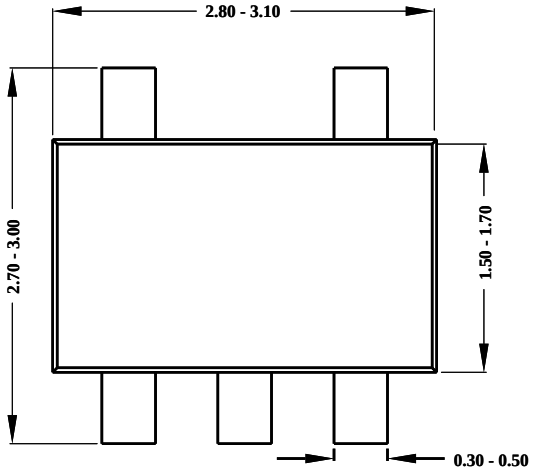
Note 2: θJA is measured in the natural convection at T_A = 25°C on a two-layer Silergy Evaluation Board.

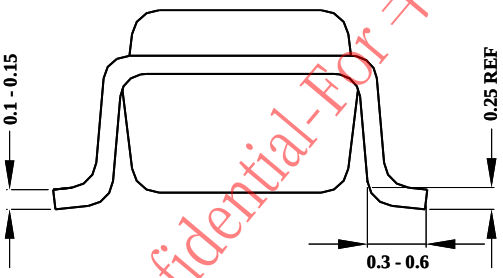
Note 3: The device is not guaranteed to function outside its operating conditions.

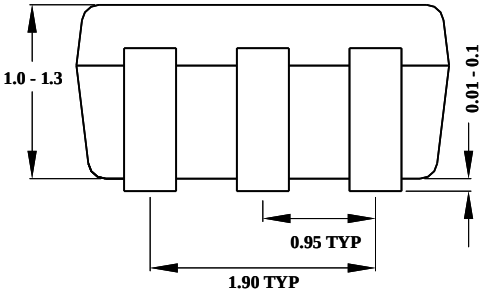
SOT23-5 Package outline & PCB layout design



Recommended Pad Layout

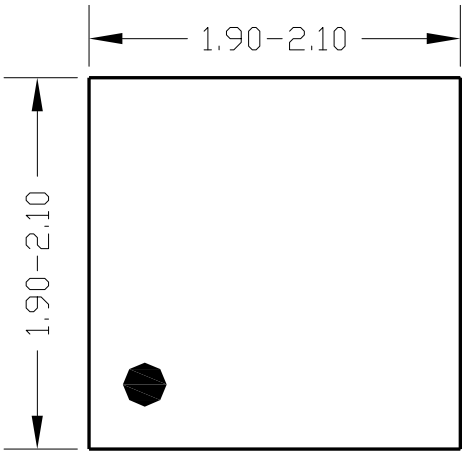




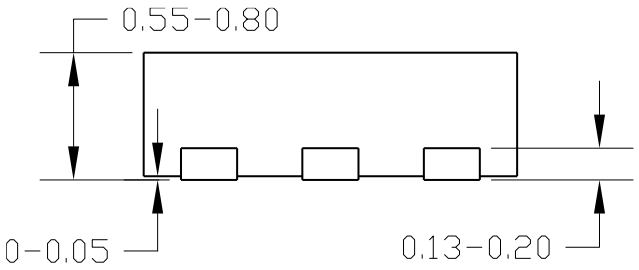


Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

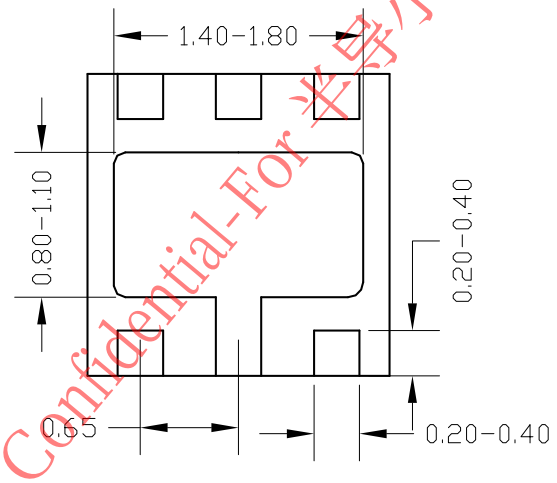
DFN2x2-6 Package outline



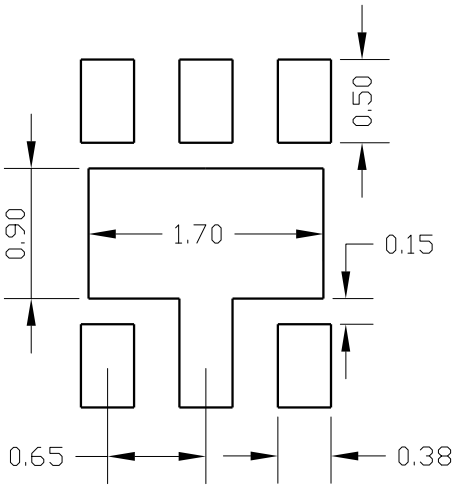
Top View



Side View



Bottom View



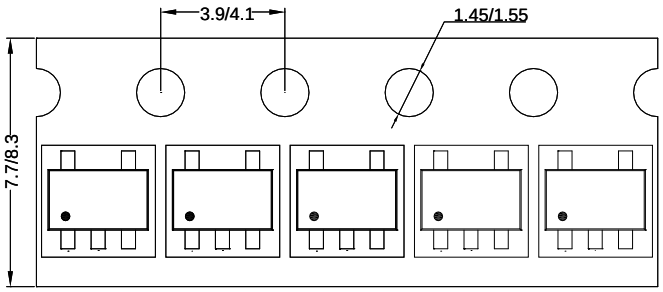
Recommended PCB layout

Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

Taping & Reel Specification

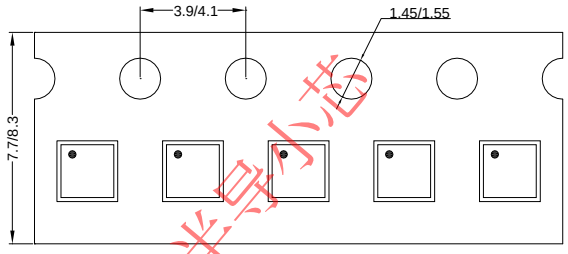
1. Taping orientation

SOT23-5



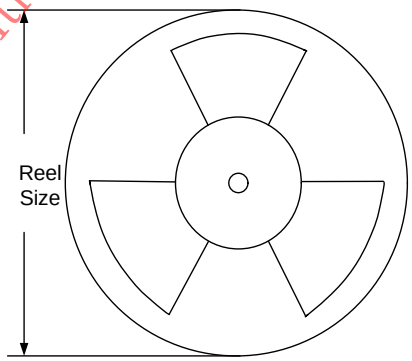
Feeding direction →

2. DFN2x2 taping orientation



Feeding direction →

3. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-5	8	4	7"	280	160	3000
DFN2x2	8	4	7"	400	160	3000

4. Others: NA