SY6924

High Efficiency, 2.5A, Multi-Cell Li-Ion Battery Charger

General Description

SY6924 is a 4-14V input, 2.5A multi-cell Li-Ion battery step-down charger. The charge current up to 2.5A can be programmed by using the external resistor for different portable applications. It also has a programmable charge timeout and adaptive input power limit for safety battery charge operation. It consists of 16V rating reverse blocking FET and power switching FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

SY6924 along with small QFN3×3 footprint provides small PCB area application.

Ordering Information

SY6924 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6924QDC	QFN3×3-16	

Features

- Integrated Synchronous Buck and Reverse Blocking FET with 16V Rating
- Adaptive Input Power Limit for 4-14V Wide Input Voltage
- Maximum 2.5A Programmable Charge Current
- 4.2V and 4.35V Constant Voltage Selectable
- +/-0.5% Cell Voltage Accuracy
- Support Single-cell or Two-cell Battery Pack
- External Shutdown Function
- Input Voltage UVLO and OVP
- Thermal Fold-back Protection
- Over Temperature Protection
- Battery Short Protection
- Programmable Charge Timeout
- Charge Status Indication
- Low Profile QFN3×3 Package for Portable Applications

Applications

- Power Bank
- Cellular Telephones, PDA, MP3 Players, MP4 Players
- PSP Game Players, NDS Game Players
- Notebook

Typical Applications

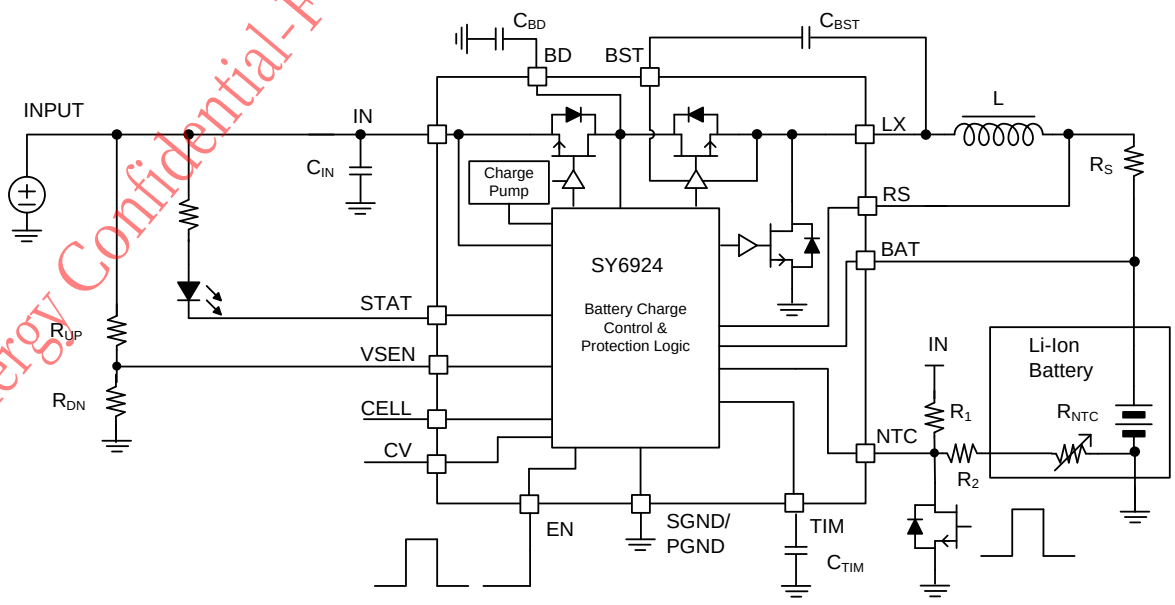
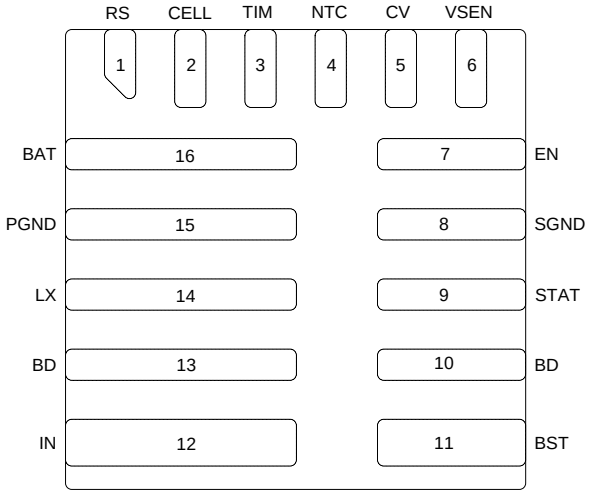


Figure1. Schematic Diagram

Pinout (top view)



(QFN3×3-16)

Top Mark: **Yn*xyz***, **(**Device code: Yn, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Description
RS	1	Charge current sense resistor positive pin. The sensed voltage drop between RS and BAT is used for charge current regulation and charge termination detection.
CELL	2	Battery voltage selection pin. Floating for two cells battery and grounding for single cell battery. CELL pin can't be pulled high to any bias voltage higher than 3.3V.
TIM	3	Charge time-out programming pin. Connect this pin with a capacitor to ground to program the time-out protection threshold. Internal current source charge the capacitor for TC mode and fast charge (CC&CV) mode's charge time limit. TC charge time limit is about 1/9 of fast charge time.
NTC	4	Battery thermal sense pin. The voltage on the NTC pin is sensed for battery thermal protection. UTP threshold is typical 76% of V_{IN} and OTP threshold is typical 45% of V_{IN}. NTC pin also can be used for the adaptive input power limit reference refresh. The adaptive input power limit threshold will be refreshed when NTC is pulled low for more than 100ms. SY6924 sets the charge current to the trickle value; the IC will refresh the adaptive input power limit threshold according the input voltage. For higher than 6V input, the IC will clamp the input voltage at V_{IN}-0.6V by regulating the duty cycle of Buck converter. For lower than 6V input, the clamped input voltage is set by VSEN pin.
CV	5	Battery CV voltage selection pin.
VSEN	6	Input voltage sense pin for adaptive input power limit. If the voltage drops to internal 1.19V reference voltage, the V_{IN} will be clamped to setting value and input current will be limited.
EN	7	Enable control pin. High logic for enable on and low logic for enable off.
SGND	8	Signal ground pin.

STAT	9	Charge status indication pin. Open drain pin. Pull high to IN thru a LED to indicate the charge in process. When the charge is done, LED is off.
BD	10, 13	Connect to the drain of internal blocking FET. Bypass at least a 10μF ceramic cap to GND.
BST	11	Boot-strap pin. Supply main FET's gate driver. Decouple this pin to LX with a 0.1μF ceramic cap.
IN	12	DC power input pin. Connect a MLCC from this pin to ground to decouple high harmonic noise. This pin has OVP and UVLO function to make the charger operate within safe input voltage area.
LX	14	Switch node pin. Connect to external inductor.
PGND	15	Power ground pin.
BAT	16	Battery voltage sense pin.

Absolute Maximum Ratings (Note 1)

IN, BAT, LX, NTC, STAT, BD, EN, CV, VSEN ---------- 18V
TIM, CELL---------- 4V
BST-LX Voltage ---------- 4V
RS ---------- BAT-0.3~BAT+0.3V
LX Pin Current Continuous ---------- 5A
Power Dissipation, P_D @ T_A = 25℃, QFN3×3---------- 2.1W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 48 ℃/W
θ_{JC} ---------- 4 ℃/W
Junction Temperature Range ---------- -40℃ to 125℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃

Recommended Operating Conditions (Note 3)

IN ---------- 4V to 14V
BAT, LX, NTC, STAT, BD, EN, CV, VSEN----------0V to16V
TIM, CELL---------- 0V to 3.3V
BST-LX Voltage ---------- 0V to 3.3V
RS ---------- BAT-0.25~BAT+0.25V
LX Pin Current Continuous ---------- 4.5A
Junction Temperature Range ---------- -40℃ to 100℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

T_A=25℃, V_{IN}=5V, GND=0V, C_{IN}=10μF, L=2.2μH, R_S=10mΩ, C_{TIM}=330nF, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Bias Supply (V_{IN})						
Supply Voltage Operation Range	V_{IN}		4		14	V
Input Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising and measured from IN to ground			4	V
Input Voltage Lockout Hysteresis	ΔV_{UVLO}	Measured from IN to ground		0.2		V
Input Over Voltage Protection	V_{IN_OVP}	V_{IN} rising and measured from IN to ground	13.5			V
Input Over Voltage Protection Hysteresis	ΔV_{OVP}	Measured from IN to ground		0.5		V
Quiescent Current						
Battery Discharge Current	I_{BAT}	V_{IN} absent or EN=Low		5	10	μA
Input Quiescent Current	I_{IN}	Disable charge		0.8	1.1	mA
Oscillator and PWM						
Switching Frequency	f_{SW}			500		kHz
Power MOSFET						
$R_{DS(ON)}$ of Main N-FET	R_{NFET_M}			30		mΩ
$R_{DS(ON)}$ of Rectified N-FET	R_{NFET_R}			55		mΩ
$R_{DS(ON)}$ of Blocking N-FET	R_{NFET_B}			45		mΩ
Voltage Regulation						
Battery Charge Voltage	V_{BAT_REG}	1-cell battery, V_{CV}<0.4V	4.179	4.2	4.221	V
		1-cell battery, V_{CV}>1.5V	4.328	4.35	4.371	
		2-cell battery, V_{CV}<0.4V	8.358	8.4	8.442	
		2-cell battery, V_{CV}>1.5V	8.656	8.7	8.744	
Recharge Threshold Refer to V_{BAT_REG}	ΔV_{RCH}	1-cell battery	50	100	150	mV
		2-cell battery	100	200	300	
Trickle Charge Rising Edge Threshold	V_{TRK}	1-cell battery	2.7	2.8	2.9	V
		2-cell battery	5.4	5.6	5.8	
Adaptive Input Current REF Modify						
NTC Voltage Threshold for Adaptive Input Current Reference Refresh	V_{NTC}	NTC falling edge	0.4			V
NTC Low Time to Enable the Adaptive Input Current Refresh	t_{DET}	Low pulse width		100		ms
Charge Current						
Charge Current Accuracy for Constant Current Mode	I_{CC}	I_{CC}=25mV/R_S	-10%		10%	
Charge Current Accuracy for Trickle Current Mode	I_{TC}	I_{TC}=2.5mV/R_S	-50%		50%	
Termination Current	I_{TERM}	I_{TERM}=2.5mV/R_S	-50%		50%	
Output Voltage OVP						
Output Voltage OVP Threshold	V_{O_OVP}		105%	110%	115%	V_{BAT_REG}
Adaptive Input Power Limit Reference						
Reference for Adaptive Input Power Limit	V_{SEN}		1.16	1.19	1.22	V
The Adaptive Input Power Limit Reference is V_{IN}-ΔV_{AICL}	ΔV_{AICL}	NTC pull low than 100ms and V_{IN} is higher than 6V		600		mV

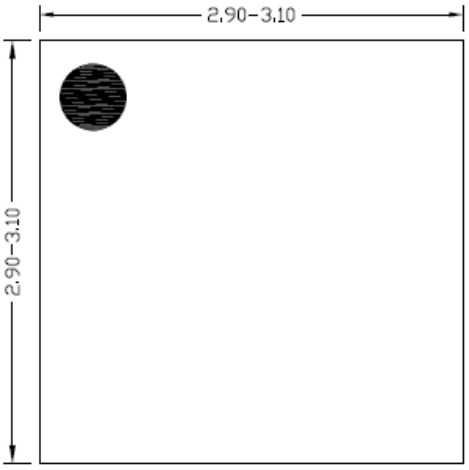
Timer						
Trickle Current Charge Timeout	t_{TC}		0.36	0.5	0.64	hour
Constant Current Charge Timeout	t_{CC}		3.5	4.5	5.5	hour
Charge Mode Change Delay Time	t_{MC}			30		ms
Termination Delay Time	t_{TERM}			30		ms
Recharge Time Delay	t_{RCHG}			30		ms
Short Circuit Protection						
Output Short Protection Threshold, Falling Edge	V_{SHORT}		1.7	2.00	2.3	V
Auto Shut Down						
Auto Shutdown Voltage Threshold	V_{ASD}	V_{IN} fall, measured from IN to BAT	40	110	180	mV
Auto Shutdown Voltage Threshold Hysteresis	ΔV_{ASD}	V_{IN} rise, measured from IN to BAT		65		
Logical Control						
High Level Logic for Enable Control	V_{ENH}		1.5			V
Low Level Logic for Enable Control	V_{ENL}				0.4	V
High Level Logic for CV	V_{CVH}		1.5			V
Low Level Logic for CV	V_{CVL}				0.4	V
Battery Thermal Protection NTC						
Under Temperature Protection	V_{NTC_UTP}		75%	76%	77%	V_{IN}
Under Temperature Protection Hysteresis	$V_{NTC\_UTP\_HYS}$	Falling edge		5%		
Over Temperature Protection	V_{NTC_OTP}		44%	45%	46%	
Over Temperature Protection Hysteresis	$V_{NTC\_OTP\_HYS}$	Rising edge		1.5%		
Thermal Fold-back and Thermal Shutdown						
Thermal Fold-back Threshold	T_{Fold}			120		℃
Thermal Fold-back Hysteresis Falling Edge	$T_{FoldHYS}$			20		℃
Thermal Fold-back Ratio	I_{Fold}			0.25		I_{CC}
Thermal Shutdown Temperature	T_{SD}	Rising threshold		160		℃
Thermal Shutdown Temperature Hysteresis	T_{SDHYS}			30		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

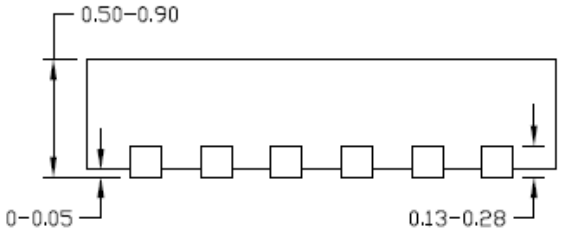
Note 2: θ_{JA} is measured in the natural convection at T_A = 25℃ on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

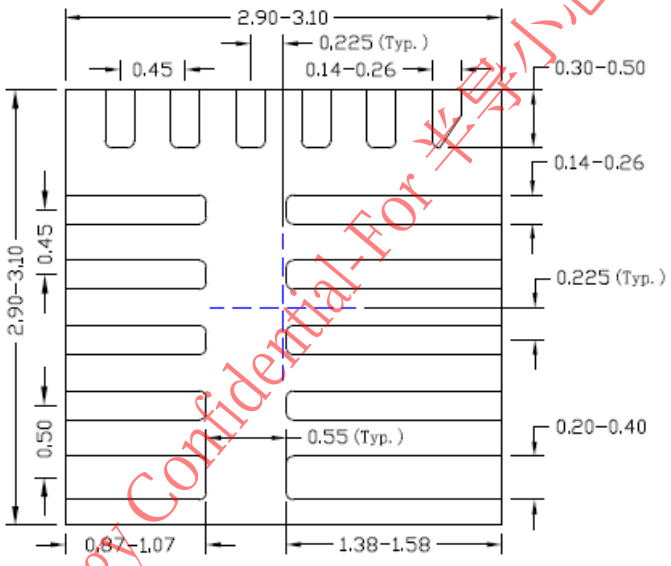
QFN3×3-16 Package Outline Drawing



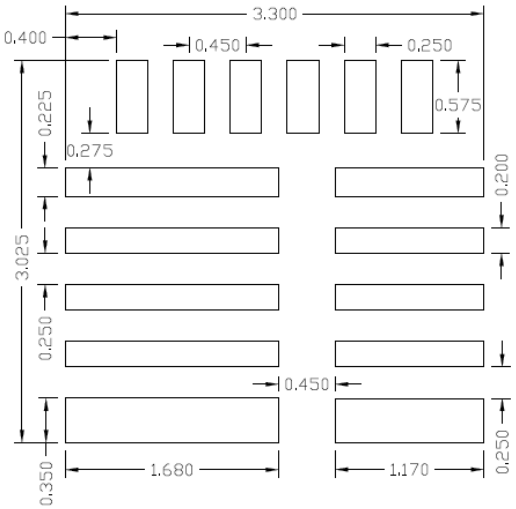
Top View



Side View



Bottom View



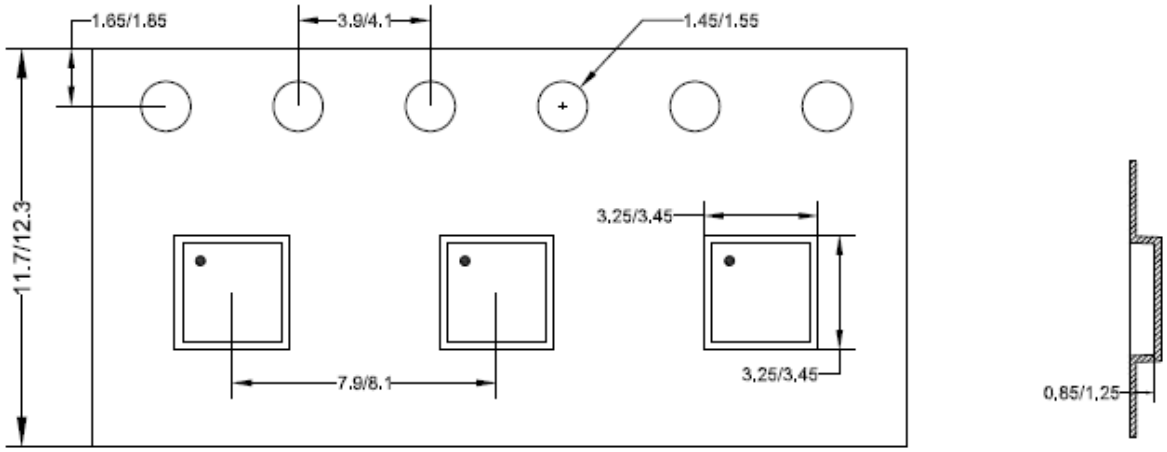
Recommended PCB Layout
(Reference Only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

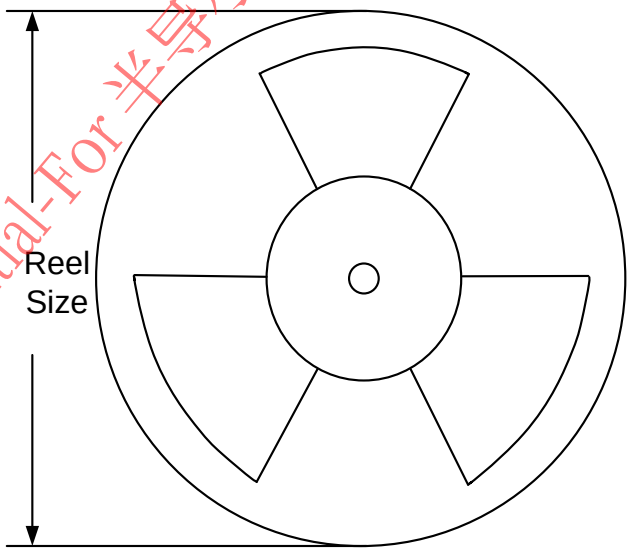
1. Taping orientation

QFN3x3



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3x3	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Mar.26, 2020	Revision 0.9B	Change "V_{NTC_UTP}" min value from 74% to 75%, typical value from 75% to 76% , max value from 76% to 77%
,Nov.16, 2017	Revision 0.9A	1. Change "V_{NTC_UTP}" min value from 70% to 74%, max value from 80% to 76%. 2. Change "V_{NTC_OTP}" min value from 43% to 44%, max value from 47% to 46%. 3. In Page 10, Change from "Define KUT, KUT =70~80%" to "Define KUT, KUT =74~76%", change from "Define KOT, KOT =43~47%" to "Define KOT, KOT =44~46%". 4. In page 10, chage the formula from $R_S = \frac{25}{I_{CC}}$ to $R_S = \frac{25mV}{I_{CC}}$ 5. In page 11, change the formula from "CTIM=2×10-11TCC" to "CTIM=2×10-11S×TCC".
Aug. 9, 2017	Revision 0.9	Initial Release

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