AN_SY7080

0.9V Minimum Input and 4V Maximum Output 1.8A Peak Current Synchronous Boost with Output Disconnect

General Description

SY7080 is a 1.2MHz fixed frequency, Current mode, high efficiency synchronous boost regulator that converts down to 0.9V input into up to 4V output voltage. It adopts very low Rdson N-MOS for the main switch and P-MOS for the synchronous switch, so no external Schottky didode is required, and the system efficiency is improved. It can disconnect the output during the shutdown operation. The SY7080 intended for systems that are typically operated from a single or dual-cell nickel-cadmium(NICd), mickel-metal hydride (NiMH), or alkaline battery.

Ordering Information

SY7080□(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY7080ABC	SOT23-6	----

Features

- 0.9V to 4V wide input range
- 4V max output voltage
- 1.8A internal switch
- Up to 95% efficiency
- < 1uA shut down current
- 1.2MHz switching frequency
- Minimum on time: 80ns typical
- Minimum off time: 60ns typical
- Output disconnect at shutdown
- Low $R_{DS(ON)}$ (main switch/synchronous switch) at 3.3V output: 90/200mΩ
- Compact SOT23-6

Applications

- LiIon or LiPolymer powered Cell Phones, DSCs, PMP, GPS.
- Alkaline battery powered electronic equipment.
- wireless mouse.

Typical Applications

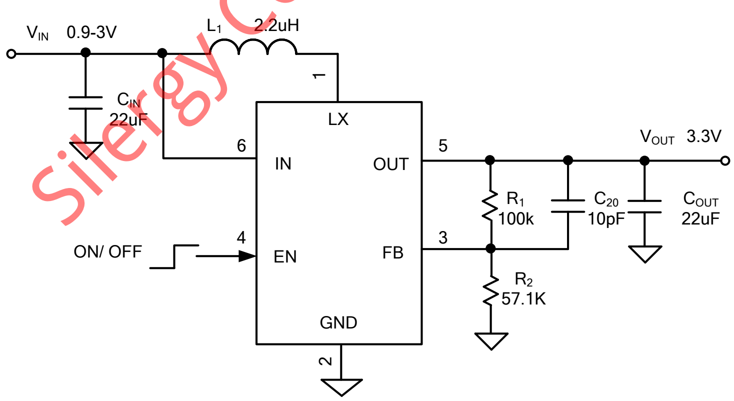


Figure 1. Schematic Diagram

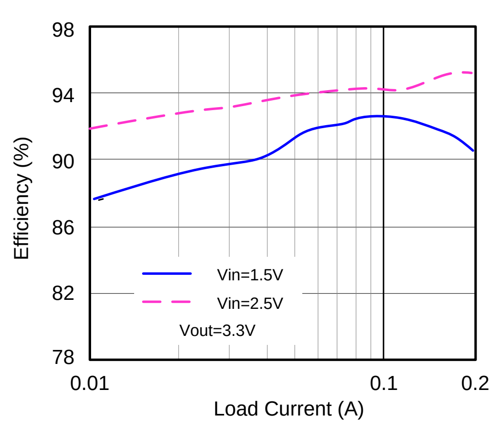
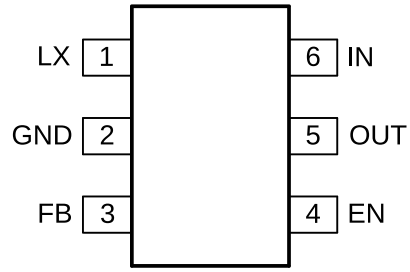


Figure 2. Efficiency vs. Load Current

Pinout (top view)



(SOT23-6)

Top mark: **EE*xyz*** (Device code:EE., ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
IN	6	Power input pin.
GND	2	Ground pin
EN	4	Enable pin. Do not float this pin.
OUT	5	Voltage output pin.
LX	1	Inductor node. Connect an inductor between IN pin and LX pin
FB	3	Feedback pin. Connect a resistor R_1 between OUT and FB, and a resistor R_2 between FB and GND to program the output voltage. $V_{OUT}=1.2V*(R_1/R_2+1)$

Absolute Maximum Ratings (Note 1)

All Pins to GND--- 4.5V
Power Dissipation, P_D @ T_A = 25 ℃ SOT23-6 --- 0.6W
Package Thermal Resistance (Note 2)
θ_{JA} --- 170 ℃/W
θ_{JC} --- 130 ℃/W
Junction Temperature Range --- 125 ℃
Lead Temperature (Soldering, 10 sec.) --- 260 ℃
Storage Temperature Range -- -65 ℃ to 150 ℃

Recommended Operating Conditions (Note 3)

IN -- 0.9V to 4V
EN -- 0V to V_{OUT}+0.3V
All other pins --- 0-4V
Junction Temperature Range --- -40 ℃ to 125 ℃
Ambient Temperature Range --- -40 ℃ to 85 ℃

Electrical Characteristics

(V_{IN} =2.5V, V_{OUT}=3.3V, I_{OUT}=100mA, T_A = 25 ℃ unless otherwise specified)

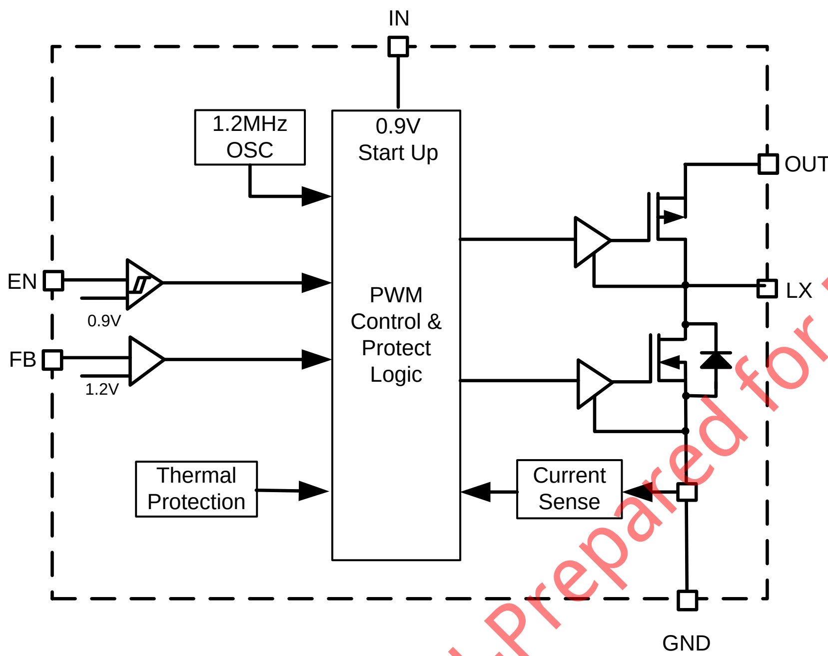
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Minimum Input Voltage	V_{IN}	R_{LOAD}=2kΩ		0.9		V
Output Voltage Range	V_{OUT}		2.5		4	V
Quiescent Current	I_Q	EN=high, V_{FB}=1.32V		65		μA
Shutdown Current	I_{SHDN}	EN=0V			1	μA
EN Rising Threshold	V_{ENH}		0.9			V
EN Falling Threshold	V_{ENL}				0.4	V
Low Side Main FET R_{ON}	$R_{DS(ON)1}$			90		mΩ
Synchronous FET R_{ON}	$R_{DS(ON)2}$			200		mΩ
Main FET Current Limit	I_{LIM1}		1.5	1.8		A
Switching Frequency	Fsw		1.0	1.2	1.4	MHz
Min On Time				80		nS
Max Duty Cycle				90		%
Feedback Reference Voltage	V_{REF}		1.164	1.2	1.236	V
FB Input Current	I_{FB}		-50		50	nA
Thermal Shutdown Temperature	T_{SD}			150		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25 ℃ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

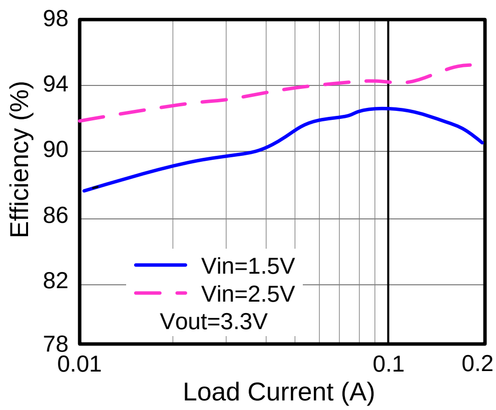
Note 3: The device is not guaranteed to function outside its operating conditions.

Function Block

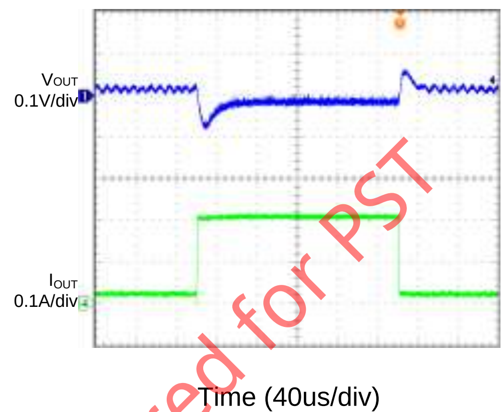


Typical Performance Characteristics

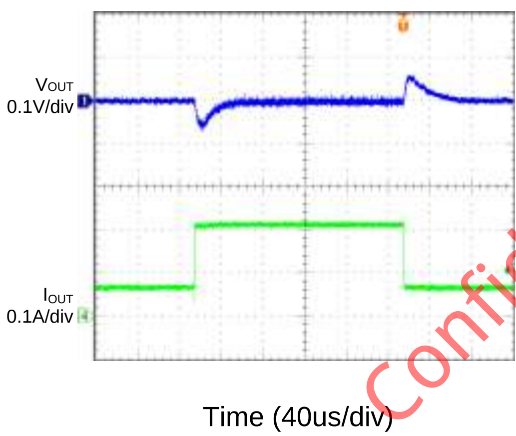
Efficiency vs Load Current



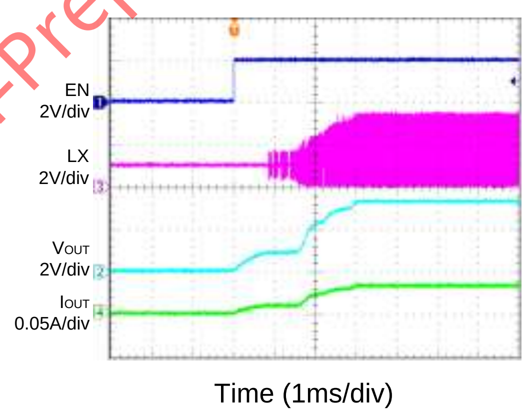
Load Transient
(VIN=1.5V, VOUT=3.3V, Iload=0.03-0.2A)



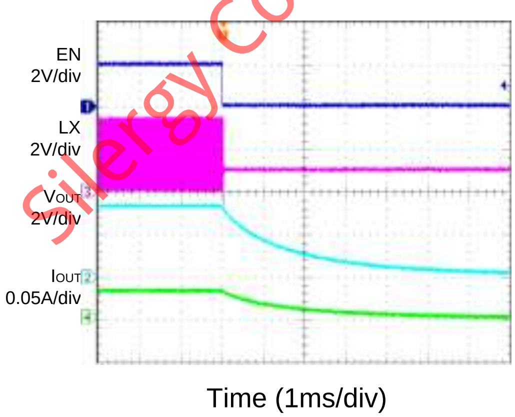
Load Transient
(VIN=1.5V, VOUT=3.3V, Iload=0.06-0.2A)



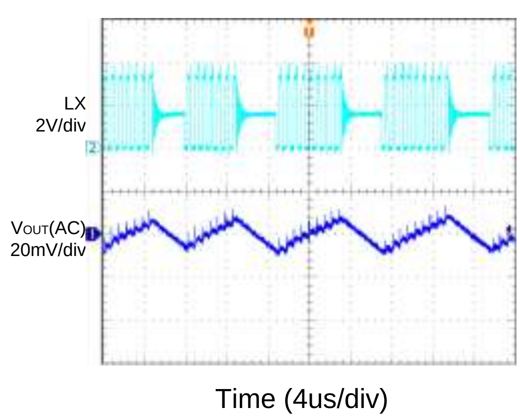
Startup from Enable
(VIN=0.9V, VOUT=3.3V, Rload=100Ω)



Shutdown from Enable
(VIN=0.9V, VOUT=3.3V, Rload=100Ω)

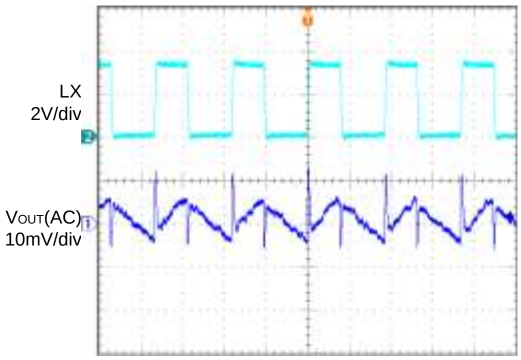


Output Ripple
(VIN=1.5V, VOUT=3.3V, Iload=30mA)



Output Ripple

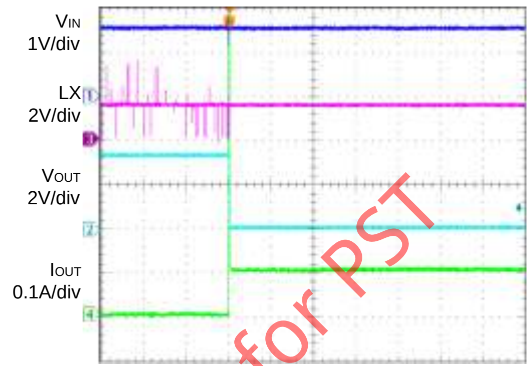
(V_{IN}=1.5V, V_{OUT}=3.3V, I_{load}=200mA)



Time (400ns/div)

Open Load to Short

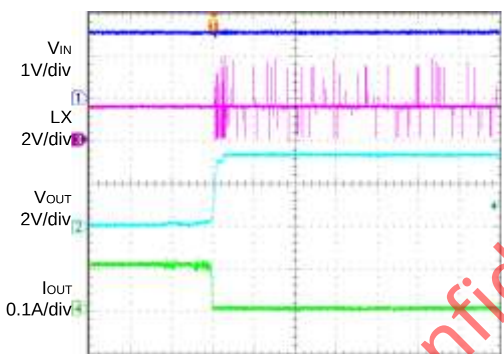
(V_{IN}=1.5V, V_{OUT}=3.3V)



Time (4ms/div)

Short Recovery

(V_{IN}=1.5V, V_{OUT}=3.3V)



Time (4ms/div)

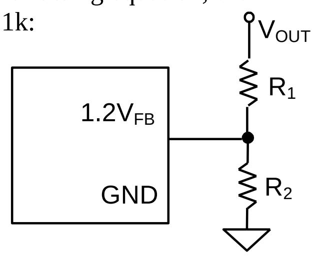
Applications Information

Because of the high integration in the SY7080 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R1 and R2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10k and 1M is recommended for both resistors. If Vout is 3.3V, R1=100k is chosen, using following equation, then R2 can be calculated to be 57.1k:

$$R_2 = \frac{1.2V}{V_{OUT} - 1.2V} R_1.$$



Input capacitor CIN:
The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{2\sqrt{3} \cdot L \cdot F_{SW} \cdot V_{OUT}}$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 22uF low ESR ceramic capacitor is recommended.

Output capacitor COUT:
The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 6.3V rating and greater than 22uF capacitance.

Output inductor L:
There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where F_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.
The SY7080 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,\,MAX} + \frac{V_{IN}}{V_{OUT}} \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mohm to achieve a good overall efficiency.

Enable Operation
Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY7080 shutdown current drops to lower than 1uA, Driving the EN pin high (> 0.9V) will turn on the IC again.

Layout Design:
The layout design of SY7080 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, L, R_1 and R_2.

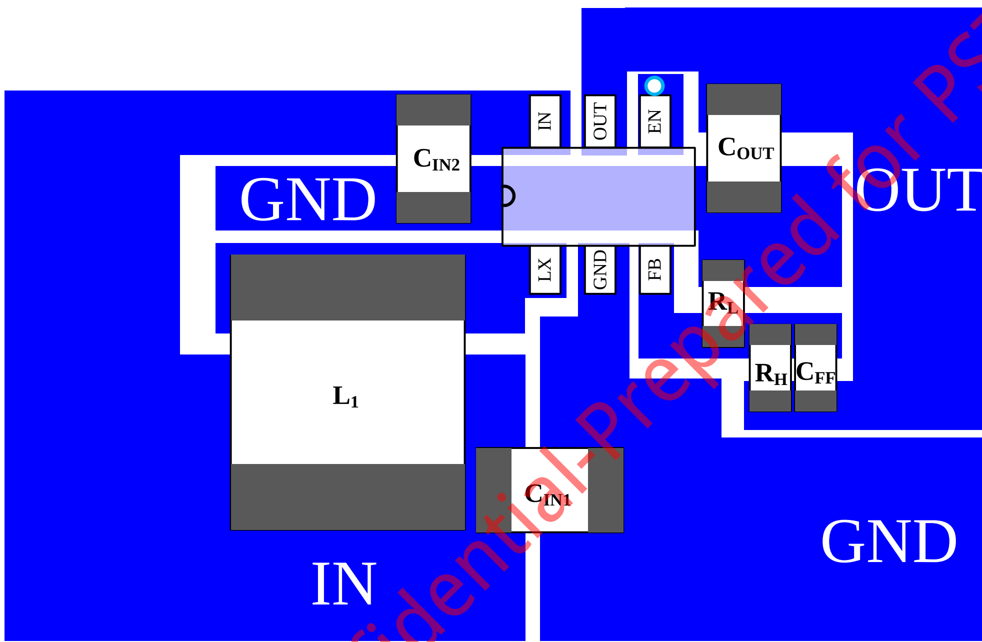
1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

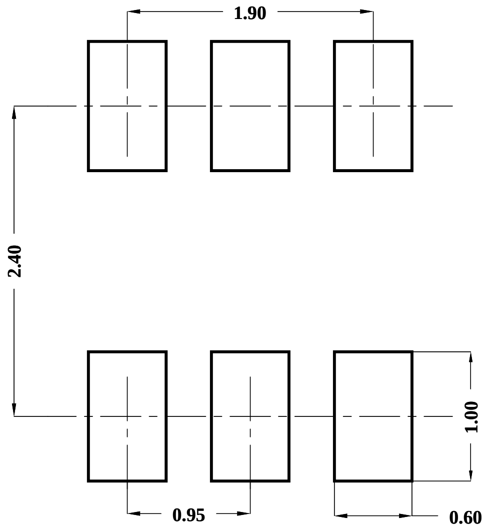
3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) The components R_1 and R_2, and the trace connecting to the FB pin must not be adjacent to the LX net on the PCB layout to avoid the noise problem.

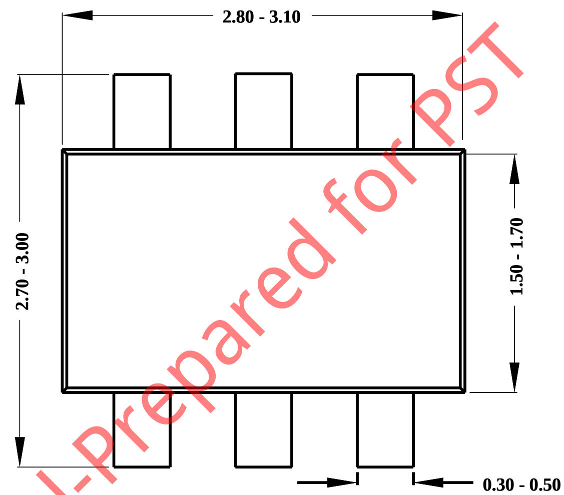
5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

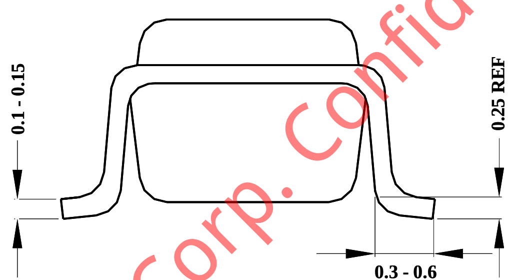


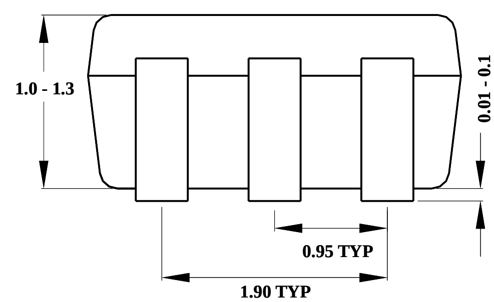
SOT23-6 Package outline & PCB layout design



Recommended Pad Layout



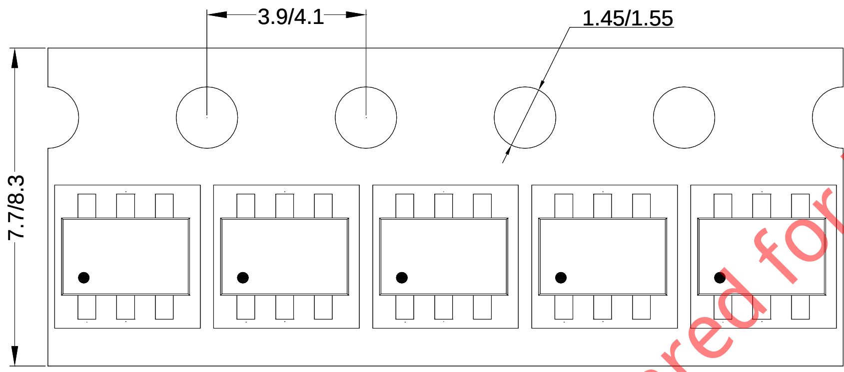




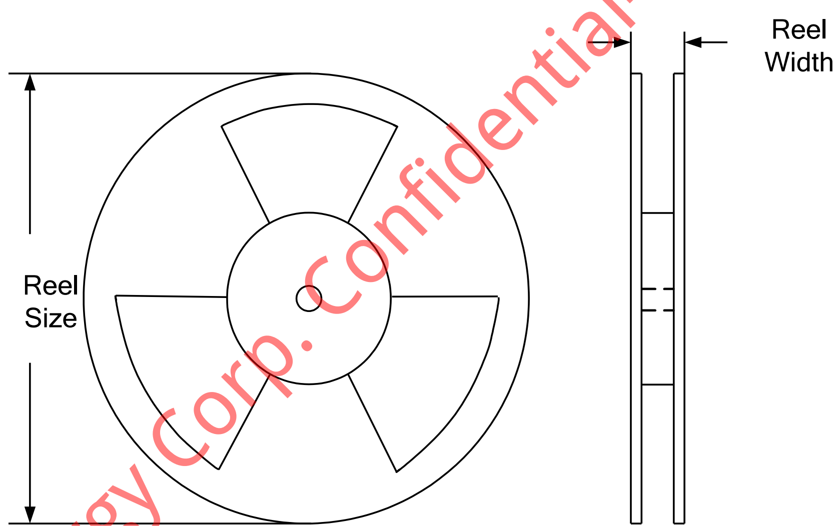
Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

Taping & Reel Specification

1. SOT23-6 (SOT26)



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7"	8.4	280	160	3000

3. Others: NA

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