SY8816

High Efficiency 6V, 6A, 1.2MHz Synchronous Step Down Regulator

General Description

SY8816 is a high efficiency high frequency synchronous step down DC/DC regulator capable of delivering up to 6A output current. It operates over a wide input voltage range from 2.75V to 6V. It integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. High integrated solution and DFN2x2-8 package perform the optimized BOM cost and reduce external component part count. Low input and output voltage ripple, small external inductor and capacitor sizes, small PCB layout space are achieved.

Ordering Information

SY8816 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8816DFC	DFN2x2-8	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 35/15 mΩ
- 2.75-6V Input Voltage Range
- 1.2 MHz Switching Frequency Minimizes the External Components
- Internal Soft-start Limits the Inrush Current
- Up to 94% Efficiency
- 6A Continuous Output Current Capability
- Shutdown Mode Draws<0.1μA Supply Current
- 100% Dropout Operation
- Power Good Indicator
- OCP/UVLO/OTP Protections
- RoHS Compliant and Halogen Free
- Compact Package: DFN2x2-8

Applications

- High Definition Set Top Box
- LCD TV
- Notebook PC

Typical Applications

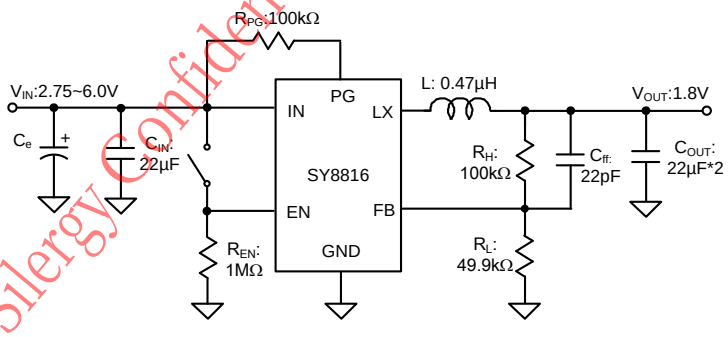


Figure 1. Schematic Diagram

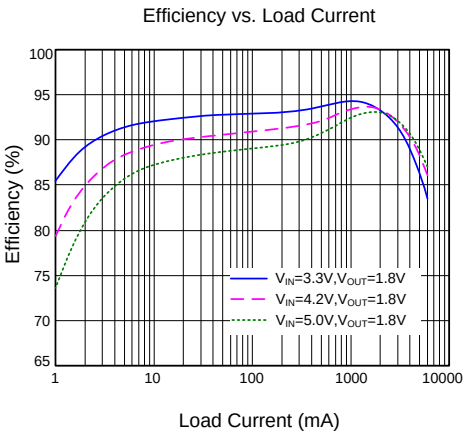
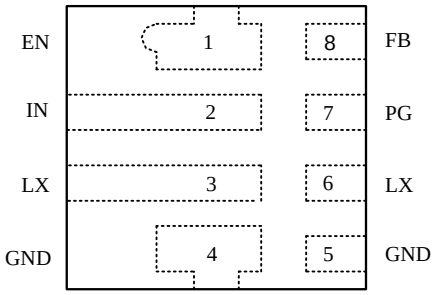


Figure 2. Efficiency vs. Load Current

Pinout (top view)



(DFN2x2-8)

Top Mark: **VW*xyz* for SY8816DFC(**device code: VW, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Description
EN	1	Enable control. Pull high to turn on. Do not leave it floating.
GND	4,5	Ground pin.
LX	3,6	Inductor pin. Connect this pin to the switching node of the inductor.
IN	2	Power input pin.
FB	8	Output feedback pin. Connect this pin to the center point of the output resistor divider(as shown in Figure.1) to program the output voltage: $V_{OUT}=0.6\times(1+R_1/R_2)$
PG	7	Power good indicator. When the output voltage exceeds 90% of regulation point, it becomes open drain. Low otherwise.

Block Diagram

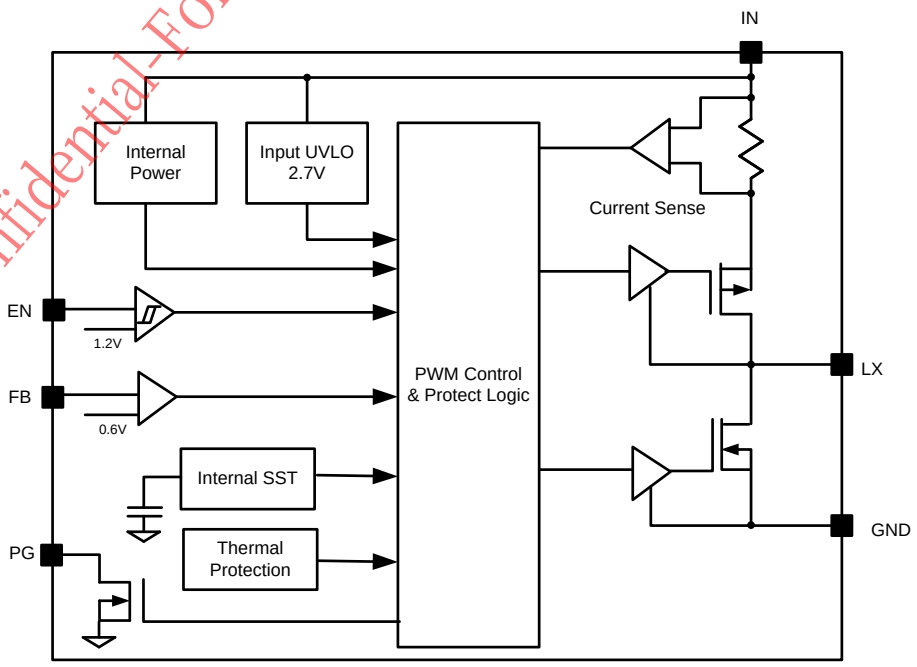


Figure 3. Block Diagram

Absolute Maximum Ratings (Note 1)

IN, LX ---------- 6.5V
All Other Pins ---------- V_{IN} + 0.6V
Power Dissipation, P_D @ T_A = 25℃ DFN2x2 ---------- 2W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 62.5℃/W
θ_{JC} ---------- 10℃/W
Junction Temperature Range ---------- 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.75V to 6.0V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 2.5V, L =0.47μH, C_{OUT} = 22μFx2, T_A = 25℃, I_{OUT} = 1A unless otherwise specified)

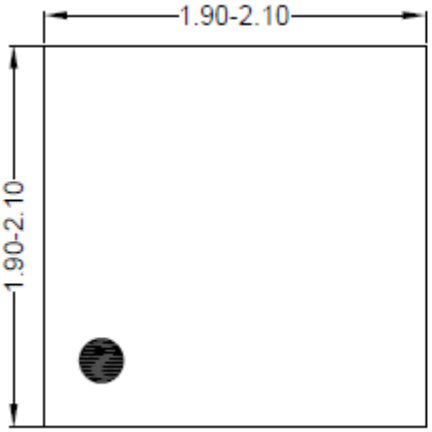
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.75		6	V
Quiescent Current	I_Q	I_{OUT}=0, EN=1, FB=105%×V_{REF}		60		μA
Shutdown Current	I_{SHDN}	EN=0		0.1	1	μA
Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
NFET $R_{DS(ON)}$	$R_{DS(ON)N}$			15		mΩ
PFET $R_{DS(ON)}$	$R_{DS(ON)P}$			35		mΩ
PFET Current Limit	I_{LIM}		7.5			A
Internal Soft-start Time	t_{SS}			0.8		ms
PGOOD Under-voltage Threshold	$V_{FB,LV}$			0.54		V
Short Circuit Protection Threshold	V_{SCP}			0.25		V
Min ON Time				60		ns
Max Duty Cycle			100			%
EN Rising Threshold	V_{ENH}		1.2			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Threshold	V_{UVLO}				2.7	V
UVLO Hysteresis	V_{HYS}			0.3		V
Oscillator Frequency	F_{OSC}			1.2		MHz
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}			15		℃
LX Node Discharge Resistance	R_{DISCHG}			50		Ω

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

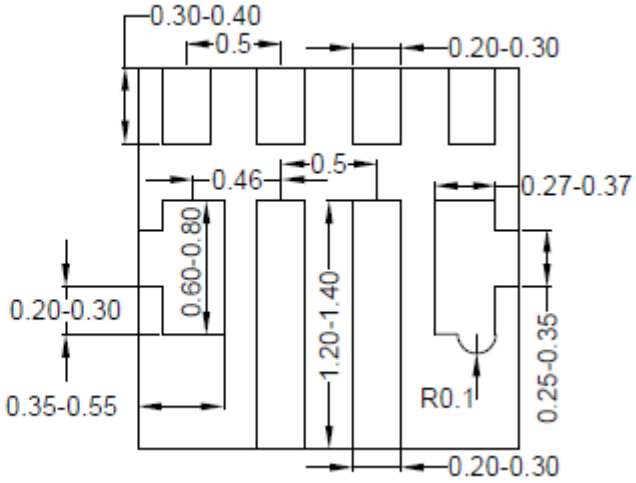
Note 2: θ_{JA} is measured in the natural convection at T_A = 25℃ on 2OZ four-layer Silergy evaluation board of JEDEC 51-3 thermal measurement standard. Paddle of DFN2x2-8 package is the case position for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

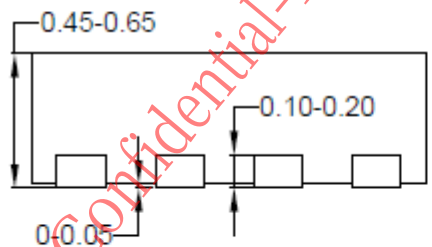
DFN2x2-8 Package Outline



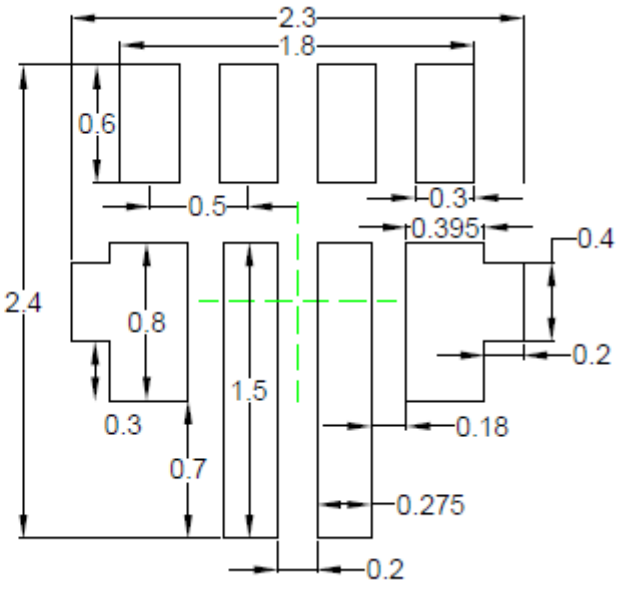
Top View



Bottom View



Side View

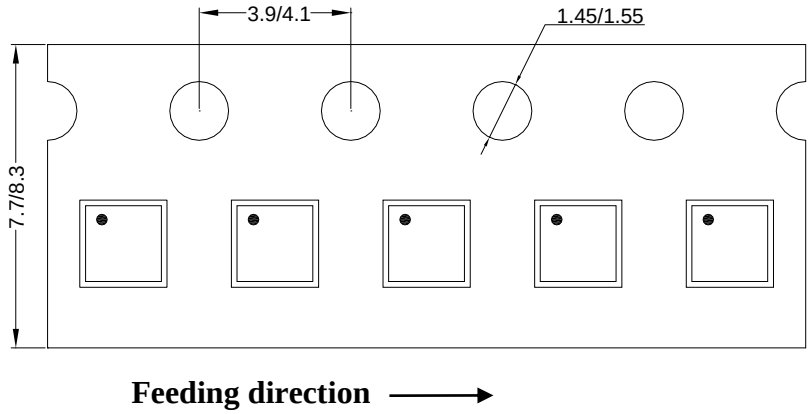


Recommended PCB Layout
（Reference only）

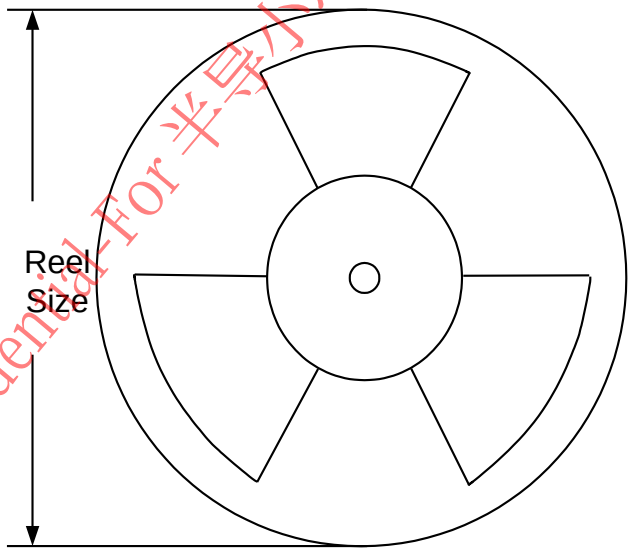
Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

1. DFN2x2



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN2x2	8	4	7"	400	160	3000

3. Others: NA