SY8859

High Efficiency 1.0MHz, 3A Synchronous Step Down Regulator

General Description

SY8859 is a high efficient 1.0MHz synchronous step down DC/DC regulator capable of delivering up to 3A output current. The SY8859 can operate over a wide input voltage range from 2.7V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The low output voltage ripple, the small external inductor and the capacitor sizes are achieved with 1.0MHz switching frequency.

Ordering Information

SY8859 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8859QWC	QFN1.5×1.5-7	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom) 85mΩ /50mΩ
- 2.7~5.5V Input Voltage Range
- 55μA Low Quiescent Current
- Ultra Fast Load Transient Speed
- High Switching Frequency 1.0MHz Minimizes the External Components
- Internal Soft-start Limits the Inrush Current
- Reliable Short Circuit Protection
- Output Auto Discharge Function
- RoHS Compliant and Halogen Free
- Compact Package: QFN1.5×1.5-7

Applications

- Smart Phone
- LCD TV
- Set Top Box
- Mini-Notebook PC
- Access Point Router

Typical Applications

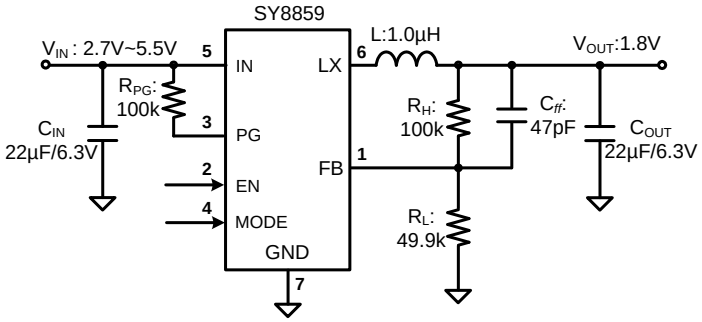


Figure1. Schematic Diagram

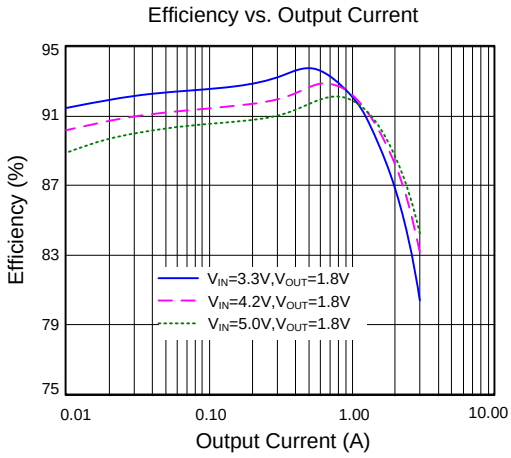
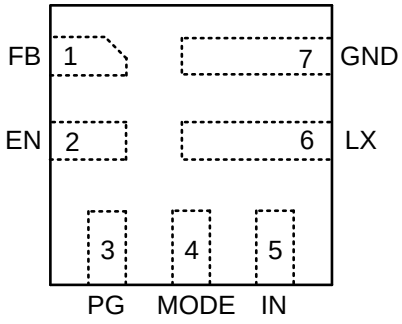


Figure2. Efficiency vs. Output Current

Pinout (Top View)



(QFN1.5×1.5-7)

Top Mark: Pr*xyz* (device code: Pr, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Pin Description
FB	1	Feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6V\times(1+R_H/R_L)$
EN	2	Enable control. Pull high to turn on. Do not leave it floating.
PG	3	Power good indicator (Open drain output). Low if the output < 90% of regulation voltage or the output >120% of regulation voltage. High otherwise. Connect a pull-up resistor to the input pin.
MODE	4	Mode control pin. Do not leave it floating. MODE=high, selected Force CCM mode operation during light load. MODE=low, selected PFM mode operation during light load.
IN	5	Input pin. Decouple this pin to GND pin with at least a 22μF ceramic capacitor.
LX	6	Inductor pin. Connect this pin to the switching node of the inductor.
GND	7	Ground pin.

Block Diagram

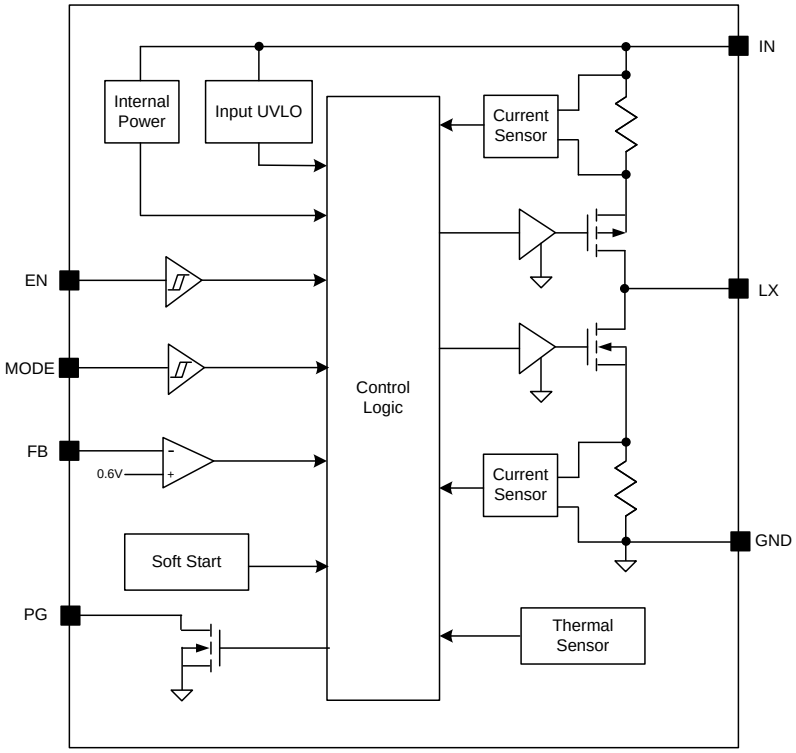


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- 6.0V
EN, PG, MODE, FB Voltage ---------- V_{IN} + 0.6V
LX Voltage ---------- -0.3V (*1) to 6V (*2)
Power Dissipation, P_D @ T_A = 25℃,
QFN1.5×1.5-7 ---------- 1.5W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 66℃/W
θ_{JC} ---------- 5℃/W
Junction Temperature Range ---------- -40℃ to 150℃
Lead Temperature (Soldering, 10 sec) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃
(*1) LX voltage tested down to -3V<40ns
(*2) LX voltage tested up to +7V<40ns

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.7V to 5.5V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(V_{IN} = 5.0V, V_{OUT} = 1.8V, L = 1.0μH, C_{OUT} = 22μF, T_A = 25℃, unless otherwise specified)

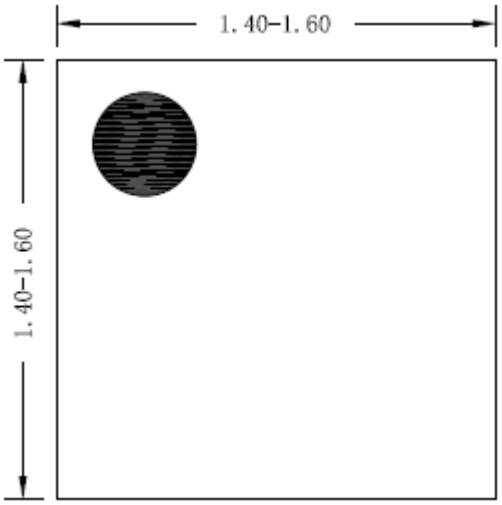
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.7		5.5	V
Input UVLO Threshold	V_{UVLO}				2.7	V
Input UVLO Hysteresis	V_{HYS}			0.18		V
Quiescent Current	I_Q	$V_{FB}=V_{REF}\times105\%$		55		μA
Shutdown Current	I_{SHDN}	EN=0V		0.1	1	μA
Feedback Reference Voltage	V_{REF}		594	600	606	mV
Output Discharge Resistance	R_{DIS}			75		Ω
Top FET R_{ON}	$R_{DS(ON)1}$			85		mΩ
Bottom FET R_{ON}	$R_{DS(ON)2}$			50		mΩ
EN Input Voltage High	$V_{EN,H}$		1.1			V
EN Input Voltage Low	$V_{EN,L}$				0.4	V
MODE Input Voltage High	$V_{MODE,H}$		1.1			V
MODE Input Voltage Low	$V_{MODE,L}$				0.4	V
PG Threshold for Under Voltage Detection	$V_{PG,UVP}$			90		$\%V_{REF}$
PG Low Delay Time for Under Voltage Detection	$t_{UVP,DLY}$			15		us
PG Threshold for Over Voltage Detection	$V_{PG,OVP}$			120		$\%V_{REF}$
PG Low Delay Time for Over Voltage Detection	$t_{OVP,DLY}$			10		us
Min ON Time	$t_{ON,MIN}$			80		ns
Maximum Duty Cycle	D_{MAX}		60			%
Turn On Delay	$t_{ON,DLY}$	from EN high to LX start switching		90		μs
Soft-start Time	t_{SS}			0.35		ms
Switching Frequency	F_{SW}	CCM		1.0		MHz
Top FET Current Limit	$I_{LMT,TOP}$		4			A
Bottom FET Current Limit	$I_{LMT,BOT}$		3			A
Output Under Voltage Protection Threshold	V_{UVP}			40		$\%V_{REF}$
Output UVP Delay	$t_{UVP,DLY}$			15		μs
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}			15		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

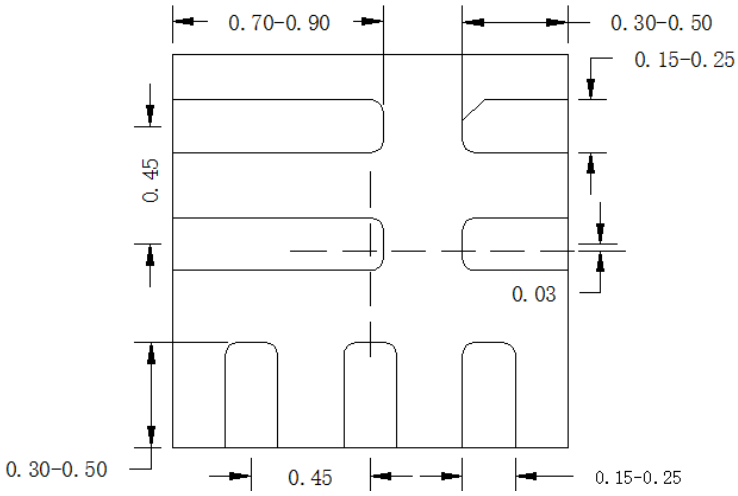
Note2: θ_{JA} of SY8859QWC is measured in the natural convection at T_A = 25℃ on a 2OZ two-layer Silergy evaluation board. Paddle of QFN1.5×1.5-7 package is the case position for SY8859QWC θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

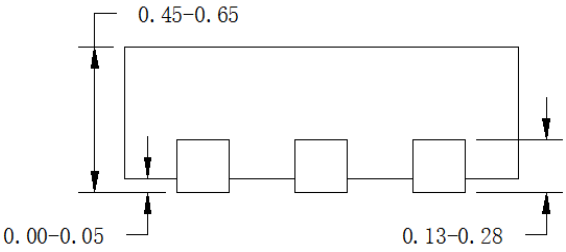
QFN1.5×1.5-7 Package Outline Drawing



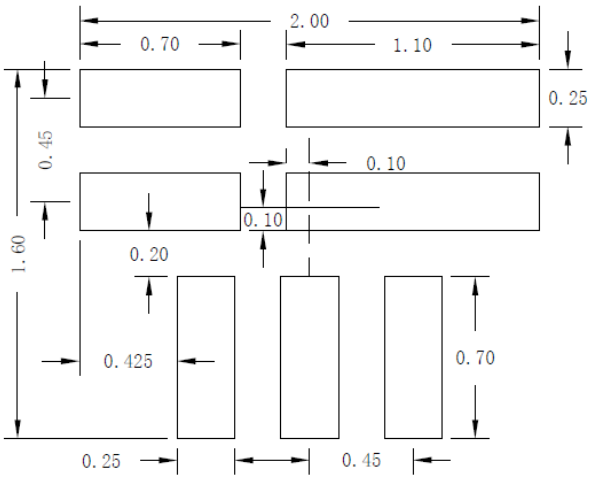
Top View



Bottom View



Side View

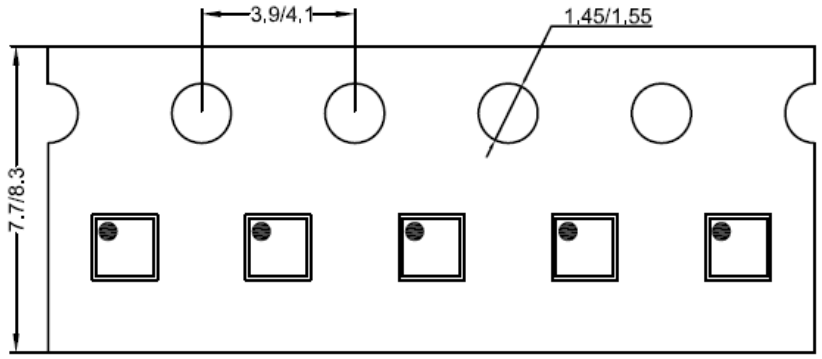


Recommended PCB Layout

Notes: **All dimension in millimeter and exclude mold flash & metal burr**

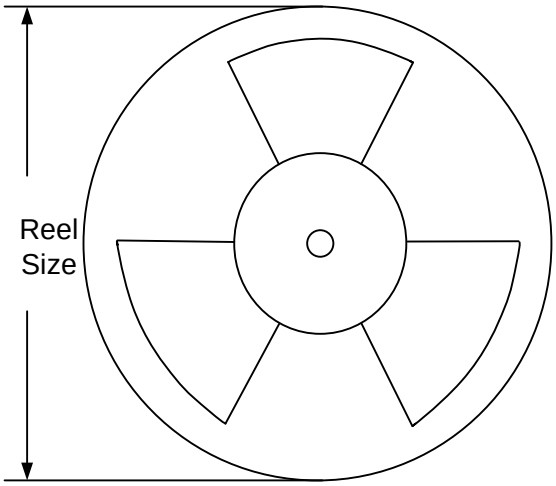
Taping & Reel Specification

1. QFN1.5×1.5 taping orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN1.5×1.5	8	4	7"	400	160	3000

3. Others: NA