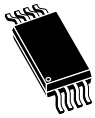
# M950x0-W M950x0-R M950x0-DF

Datasheet

## 4 Kbit, 2 Kbit and 1 Kbit serial SPI bus EEPROM with high-speed clock

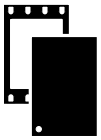
SO8N

(150 mil width)



TSSOP8

(169 mil width)



UFDFPN8 (MC)

DFN8 (2 x 3 mm)

| Product status link |
|---|
| M95040-DF |
| M95010-R |
| M95020-R |
| M95040-R |
| M95010-W |
| M95020-W |
| M95040-W |

## Features

- Compatible with the serial peripheral interface (SPI) bus
- Memory array
  - 1/2/4-Kbit (128/256/512 bytes) of EEPROM
  - Page size: 16 bytes
  - Additional write lockable page (Identification page) for M95040-DF order code
- Write
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Write protect
  - quarter array
  - half array
  - whole memory array
- Max clock frequency: 20 MHz
- Single supply voltage:
  - 2.5 V to 5.5 V for M950x0-W
  - 1.8 V to 5.5 V for M950x0-R
  - 1.7 V to 5.5 V for M95040-DF
- Operating temperature range: from -40 °C up to +85 °C
- Enhanced ESD protection
- More than 4 million write cycles
- More than 200-year data retention
- Packages RoHS-compliant and Halongen-free
  - SO8N (ECOPACK2)
  - TSSOP8 (ECOPACK2)
  - UFDFPN8 (ECOPACK2)

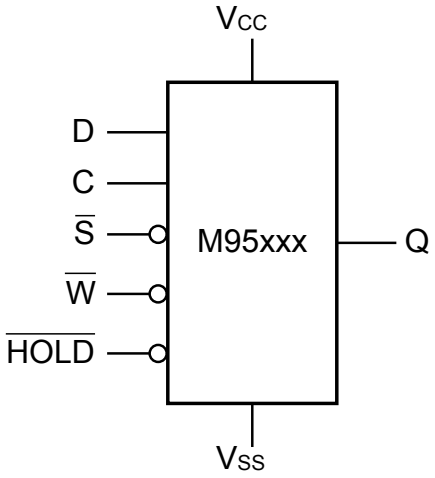
# 1 Description

The M95010/M95020/M95040 devices (M950x0) are electrically erasable programmable memories (EEPROMs) organized as 128/256/512 x 8 bits respectively, accessed through the SPI bus.

The M950x0-W can operate with a supply voltage from 2.5 V to 5.5 V, the M950x0-R can operate with a supply voltage from 1.8 V to 5.5 V and the M950x0-DF can operate with a supply voltage from 1.7 V to 5.5 V, over an ambient temperature range of -40 °C / +85 °C

The M950x0-DF offers an additional page, named the identification page (16 bytes). The identification page can be used to store sensitive application parameters that can be (later) permanently locked in read-only mode.

**Figure 1. Logic diagram**

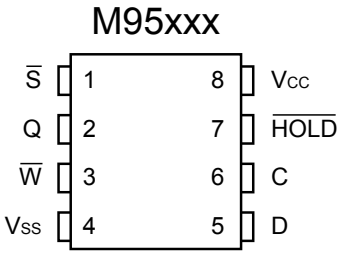



The SPI bus signals are C, D and Q, as shown in Figure 1 and Table 1. The device is selected when chip select ($\overline{S}$) is driven low. Communications with the device can be interrupted when the $\overline{HOLD}$ is driven low.

**Table 1. Signal names**

| Signal name | Function | Direction |
|---|---|---|
| C | Serial clock | Input |
| D | Serial data input | Input |
| Q | Serial data output | Output |
| $\overline{S}$ | Chip select | Input |
| $\overline{W}$ | Write protect | Input |
| $\overline{HOLD}$ | Hold | Input |
| $V_{CC}$ | Supply voltage | - |
| $V_{SS}$ | Ground | - |

**Figure 2. 8-pin package connections (top view)**

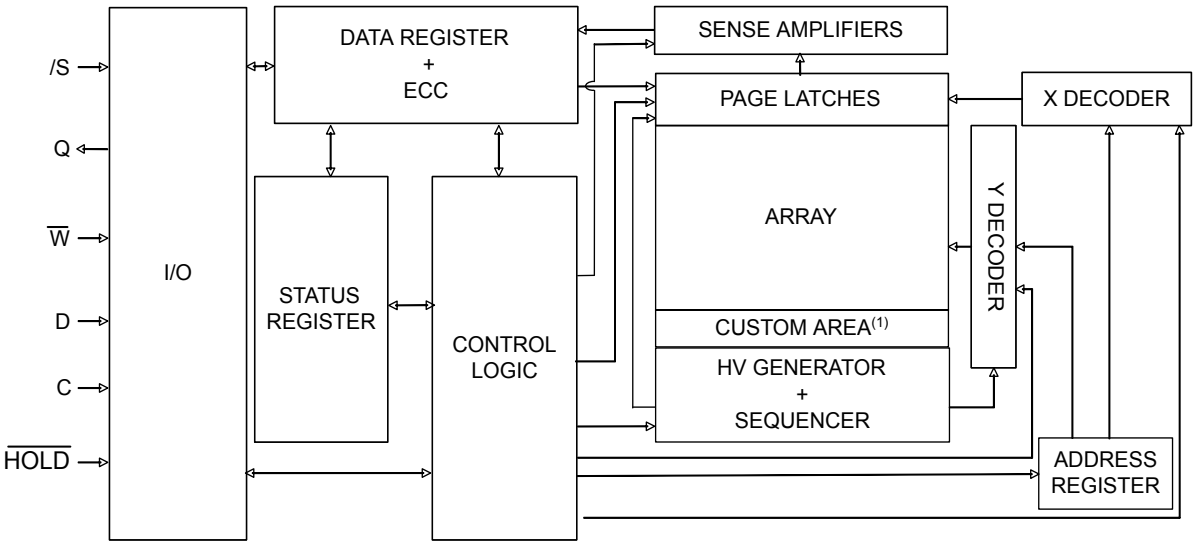



1. See Package information for package dimensions, and how to identify pin 1.

# 2 Block diagram

The memory is organized as shown in the following figure.

**Figure 3. Block diagram**




1. = Identification page

# 3 Signal description

During all operations, $V_{CC}$ must be held stable and within the specified valid range: $V_{CC}$(min) to $V_{CC}$(max).

All of the input and output signals must be held high or low (according to voltages of $V_{IH}$, $V_{OH}$, $V_{IL}$ or $V_{OL}$, as specified in Table 15 and Table 16). These signals are described next.

## 3.1 Serial data output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of serial clock (C).

## 3.2 Serial data input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of serial clock (C).

## 3.3 Serial clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at serial data input (D) are latched on the rising edge of serial clock (C). Data on serial data output (Q) change from the falling edge of serial clock (C).

## 3.4 Chip select ($\overline{S}$)

When this input signal is high, the device is deselected and serial data output (Q) is at high impedance. The device is in the standby power mode, unless an internal write cycle is in progress. Driving chip select ($\overline{S}$) low selects the device, placing it in the active power mode.

After power-up, a falling edge on chip select ($\overline{S}$) is required prior to the start of any instruction.

## 3.5 Hold ($\overline{HOLD}$)

The hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the hold condition, the serial data output (Q) is high impedance, and serial data input (D) and serial clock (C) are Don't care.

To start the hold condition, the device must be selected, with chip select ($\overline{S}$) driven low.

## 3.6 Write protect ($\overline{W}$)

This input signal controls whether the memory is write protected. When write protect ($\overline{W}$) is held low, writes to the memory are disabled, but other operations remain enabled.

Write protect ($\overline{W}$) must either be driven high or low, but must not be left floating.

## 3.7 $V_{CC}$ supply voltage

$V_{CC}$ is the supply voltage.

## 3.8 $V_{SS}$ ground

$V_{SS}$ is the reference for all signals, including the $V_{CC}$ supply voltage.

# 4 Connecting to the SPI bus

The device is fully compatible with the SPI protocol.

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The serial data input (D) is sampled on the first rising edge of the serial clock (C) after chip select ($\overline{S}$) goes low.

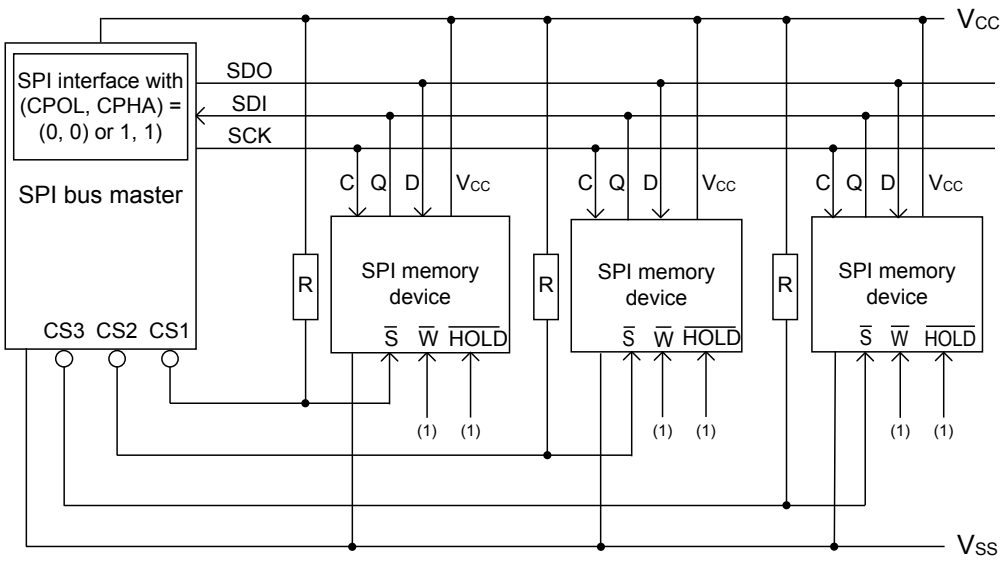
All output data bytes are shifted out of the device, most significant bit first. The serial data output (Q) is latched on the first falling edge of the serial clock (C) after the instruction (such as the read from memory array and read status register instructions) have been clocked into the device.

Figure 4 shows an example of three memory devices connected to an MCU, on an SPI bus. Only one memory device is selected at a time, so only one memory device drives the serial data output (Q) line at a time, the other memory devices are high impedance.

The pull-up resistor R (represented in Figure 4) ensures that a device is not selected if the bus master leaves the $\overline{S}$ line in the high impedance state.

In applications where the bus master may leave all SPI bus lines in high impedance at the same time (for example, if the bus master is reset during the transmission of an instruction), it is recommended to connect the clock line (C) to an external pull-down resistor so that, if all inputs/outputs become high impedance, the C line is pulled low (while the $\overline{S}$ line is pulled high): this ensures that $\overline{S}$ and C do not become high at the same time, and so, that the $t_{SHCH}$ requirement is met. The typical value of R is 100 kΩ.

**Figure 4. Bus master and memory devices on the SPI bus**




1. The Write protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, high or low as appropriate.

## 4.1 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the following two modes:

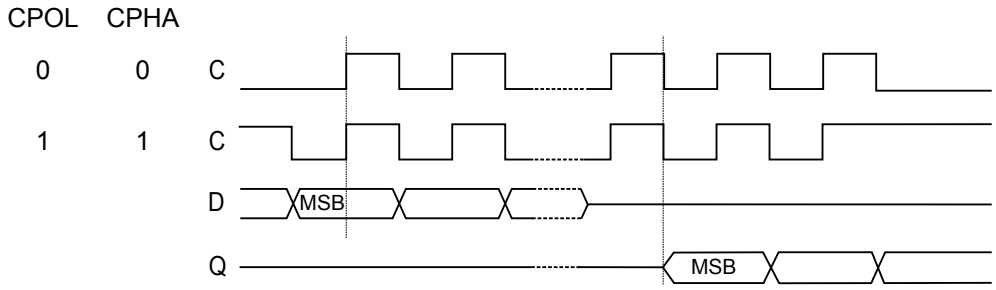
- CPOL = 0, CPHA = 0
- CPOL = 1, CPHA = 1

For these two modes, input data is latched in on the rising edge of serial clock (C), and output data is available from the falling edge of serial clock (C).

The difference between the two modes, as shown in Figure 5, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL = 0, CPHA = 0)
- C remains at 1 for (CPOL = 1, CPHA = 1)

**Figure 5. SPI modes supported**



# 5 Operating features

## 5.1 Supply voltage ($V_{CC}$)

### 5.1.1 Operating supply voltage ($V_{CC}$)

Prior to selecting the memory and issuing instructions to it, a valid and stable $V_{CC}$ voltage within the specified [$V_{CC}$(min), $V_{CC}$(max)] range must be applied (see Table 8, Table 9 and Table 10 in Section 9 DC and AC parameters). This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle ($t_W$). In order to secure a stable DC supply voltage, it is recommended to decouple the $V_{CC}$ line with a suitable capacitor (usually in the range between 10 and 100 nF) close to the $V_{CC}$ / $V_{SS}$ device pins.

### 5.1.2 Device reset

In order to prevent erroneous instruction decoding and inadvertent write operations during power-up, a power-on-reset (POR) circuit is included. At power-up, the device does not respond to any instruction until $V_{CC}$ reaches the internal reset threshold voltage(this threshold is defined in Table 15 and Table 16 as $V_{RES}$).

At power-up, when $V_{CC}$ passes over the POR threshold, the device is reset and is in the following state:

- Standby power mode
- Deselected (note that, to be executed, an instruction must be preceded by a falling edge on chip select ($\overline{S}$))
- Status register values:
  - the write enable latch (WEL) bit is reset to 0
  - the write in progress (WIP) bit is reset to 0
  - the BP1 and BP0 bits remain unchanged (non-volatile bits).

It is important to note that the device must not be accessed until $V_{CC}$ reaches a valid and stable level within the specified [$V_{CC}$(min), $V_{CC}$(max)] range, as defined in Table 8, Table 9 and Table 10.

### 5.1.3 Power-up conditions

When the power supply is turned on, $V_{CC}$ rises continuously from $V_{SS}$ to $V_{CC}$. During this time, the chip select ($\overline{S}$) line is not allowed to float but should follow the $V_{CC}$ voltage. It is therefore recommended to connect the $\overline{S}$ line to $V_{CC}$ via a suitable pull-up resistor (see Figure 4).

In addition, the chip select ($\overline{S}$) input offers a built-in safety feature, as the $\overline{S}$ input is edge-sensitive as well as level-sensitive: after power-up, the device does not become selected until a falling edge has first been detected on chip select ($\overline{S}$). This ensures that chip select ($\overline{S}$) must have been high, prior to going low to start the first operation.

The $V_{CC}$ voltage has to rise continuously from 0 V up to the minimum $V_{CC}$ operating voltage defined in Table 8, Table 9 and Table 10.

### 5.1.4 Power-down

During power-down (continuous decrease of the $V_{CC}$ supply voltage below the minimum $V_{CC}$ operating voltage defined in Table 8, Table 9 and Table 10), the device must be:

- deselected (chip select $\overline{S}$ must be allowed to follow the voltage applied on $V_{CC}$)
- in standby power mode (there must not be any internal write cycle in progress)

### 5.1.5 Active power and Standby power modes

When chip select ($\overline{S}$) is low, the device is selected, and in the active power mode. The device consumes $I_{CC}$.

When chip select ($\overline{S}$) is high, the device is deselected. If a write cycle is not currently in progress, the device then goes into the standby power mode, and the device consumption drops to $I_{CC1}$, as specified in DC characteristics (see Section 9 DC and AC parameters).

## 5.2 Hold condition

The hold ($\overline{\text{HOLD}}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

To enter the hold condition, the device must be selected, with chip select ($\overline{\text{S}}$) low.

During the hold condition, the serial data output (Q) is high impedance, and the serial data input (D) and the serial clock (C) are Don't care.

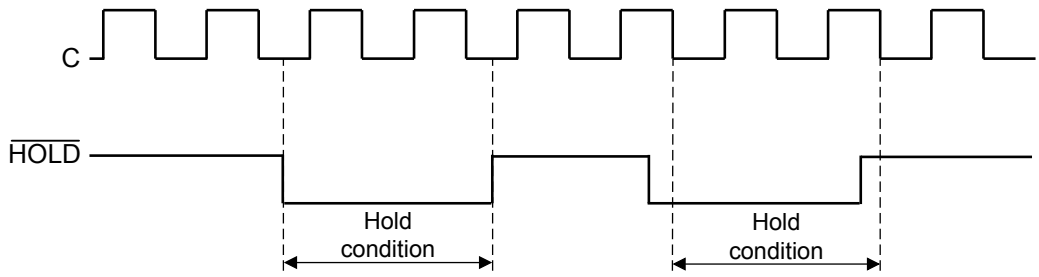
Normally, the device is kept selected for the whole duration of the hold condition. Deselecting the device while it is in the hold condition has the effect of resetting the state of the device: this mechanism can be used, if required, to reset the ongoing processes.

The hold condition starts when the hold ($\overline{\text{HOLD}}$) signal is driven low at the same time as serial clock (C) already being low (as shown in Figure 6).

The hold condition ends when the hold ($\overline{\text{HOLD}}$) signal is driven high at the same time as serial clock (C) already being low.

Figure 6 also shows what happens if the rising and falling edges are not timed to coincide with serial clock (C) being low.

**Figure 6. Hold condition activation**




## 5.3 Status register

Figure 3 shows the position of the status register in the control logic of the device. This register contains a number of status and control bits, as shown in Table 5 and as detailed in Section 6.3 Read Status register (RDSR).

## 5.4 Data protection and protocol control

To help protect the device from data corruption in noisy or poorly controlled environments, a number of safety features have been built in to the device. The main security measures can be summarized as follows:

- WEL bit is reset at power-up
- Chip select ($\overline{S}$) must rise after the eighth clock count (or multiple thereof) in order to start a non-volatile write cycle (in the memory array or in the status register)
- Accesses to the memory array are ignored during the non-volatile programming cycle, and the programming cycle continues unaffected.
- Invalid chip select ($\overline{S}$) and hold ($\overline{HOLD}$) transitions are ignored.

For any instruction to be accepted and executed, chip select ($\overline{S}$) must be driven high after the rising edge of serial clock (C) that latches the last bit of the instruction, and before the next rising edge of serial clock (C).

For this, “the last bit of the instruction” can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except in the case of RDSR and READ instructions). Moreover, the “next rising edge of CLOCK” might (or might not) be the next bus transaction for some other device on the bus.

When a write cycle is in progress, the device protects it against external interruption by ignoring any subsequent READ, WRITE or WRSR instruction as defined in Table 3 until the present cycle is complete.

**Table 2. Write-protected block size**

| Status register bits | | Protected block | Protected array addresses | | |
|---|---|---|---|---|---|
| BP1 | BP0 | | M95040 | M95020 | M95010 |
| 0 | 0 | None | None | None | None |
| 0 | 1 | Upper quarter | 180h - 1FFh | C0h - FFh | 60h - 7Fh |
| 1 | 0 | Upper half | 100h - 1FFh | 80h - FFh | 40h - 7Fh |
| 1 | 1 | Whole memory | 000h - 1FFh | 00h - FFh | 00h - 7Fh |

## 5.5 Error correction code (ECC x 1)

The error correction code (ECC x 1) is an internal logic function, which is transparent for the SPI communication protocol.

The ECC x 1 logic is implemented on each bytes of memmory array. If a single bit out of byte happens to be erroneous during a read operation, the ECC x 1 detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

# 6 Instructions

Each command is composed of bytes (MSB transmitted first), initiated with the instruction byte, as summarized in Table 3

If an invalid instruction is sent (one not contained in Table 3), the device automatically enters in a Wait state until deselected.

**Table 3. Instruction set**

| Instruction | Description | Instruction format |
|---|---|---|
| WREN | Write enable | 0000 X110(1) |
| WRDI | Write disable | 0000 X100(1) |
| RDSR | Read Status register | 0000 X101(1) |
| WRSR | Write Status register | 0000 X001(1) |
| READ | Read from memory array | 0000 $A_8$011(2) |
| WRITE | Write to memory array | 0000 $A_8$010(2) |
| RDID (3) | Read identification page | 1000 0011 |
| WRID(3) | Write identification page | 1000 0010 |
| RDLS(3) | Reads the identification page lock status | 1000 0011 |
| LID(3) | Locks the identification page in read-only mode | 1000 0010 |

1. *X = Don't Care.*
2. *For M95040, A8 = 1 for the upper half of the memory array and 0 for the lower half, while for M95010 and M95020, A8 is "Don't Care".*
3. *Available only for the M95040-DF device.*

**Table 4. Significant bits within the address bytes**

| Instruction | Bit b3 of the instruction byte | LSB address byte(1)(2) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| READ or WRITE | A8/X(3) | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| RDID or WRID | 0 | 0 | 0 | 0 | 0 | A3 | A2 | A1 | A0 |
| RDLS or LID | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

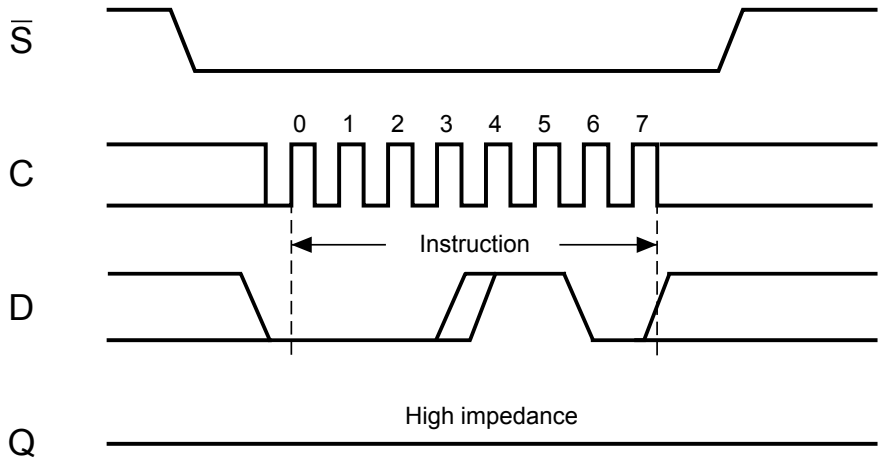
1. *A: Significant address bit.*
2. *X: bit is Don't Care.*
3. *For M95040, A8 = 1 for the upper half of the memory array and 0 for the lower half, while for M95010 and M95020, A8 is Don't Care.*

## 6.1 Write enable (WREN)

The write enable latch (WEL) bit must be set prior to a write instruction (WRITE, WRSR, WRID or LID). The only way to do this is to send a write enable instruction to the device.

As shown in Figure 7, to send this instruction to the device, chip select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on serial data input (D). The device then enters a wait state. It waits for a the device to be deselected, by chip select ($\overline{S}$) being driven high.

**Figure 7. Write enable (WREN) sequence**



## 6.2 Write disable (WRDI)

One way of resetting the write enable latch (WEL) bit is to send a write disable instruction to the device.

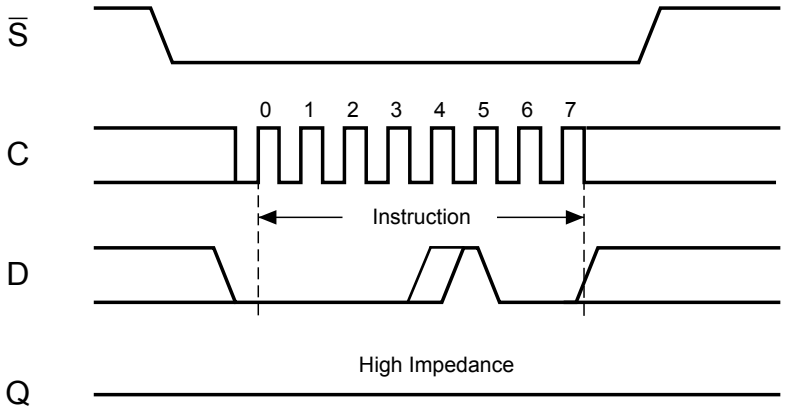
As shown in Figure 8, to send this instruction to the device, chip select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on serial data input (D).

The device then enters a wait state. It waits for a the device to be deselected, by chip select ($\overline{S}$) being driven high.

The write enable latch (WEL) bit, in fact, becomes reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion.
- Write protect ($\overline{W}$) line being held low

**Figure 8. Write disable (WRDI) sequence**



## 6.3 Read Status register (RDSR)

The read status register instruction is used to read the status Register.

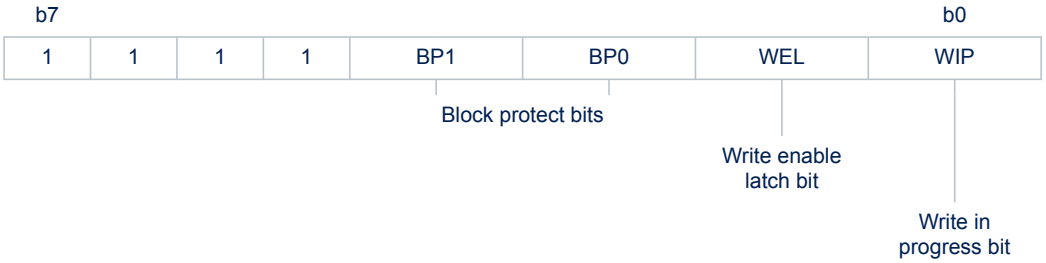
As shown in Figure 9, to send this instruction to the device, chip select ($\overline{S}$) is first driven low. The bits of the instruction byte are then shifted in, on serial data input (D). The current state of the bits in the Status register is shifted out, on serial data out (Q). The read cycle is terminated by driving chip select ($\overline{S}$) high.

The status register is always readable, even if an internal write cycle ($t_W$) is in progress. During a write status register cycle, the values of the non-volatile bits (BP0, BP1) become available when a new RDSR instruction is executed, after completion of the write cycle. On the other hand, the two read-only bits (write enable latch (WEL), write In progress (WIP)) are dynamically updated during the ongoing write cycle.

It is possible to read the status register contents continuously, as described in Figure 9.

Bits b7, b6, b5 and b4 are always read as 1. The status and control bits of the status register are as follows:

**Table 5. Status register format**




### 6.3.1 WIP bit

The write in progress (WIP) bit indicates whether the memory is busy with a write (WRITE, WRID/LID) or write status register cycle. When set to 1, such a cycle is in progress, when reset to 0, no such cycle is in progress.

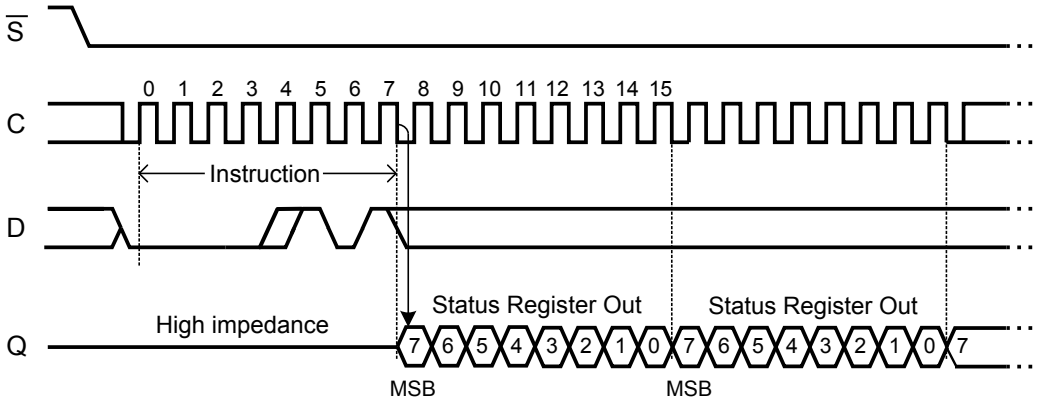
### 6.3.2 WEL bit

The write enable latch (WEL) bit indicates the status of the internal write enable latch. When set to 1, the internal write enable latch is set. When set to 0, the internal write enable latch is reset, and no write or write status register instruction is accepted.

### 6.3.3 BP1, BP0 bits

The block protect (BP1, BP0) bits are non volatile. They define the size of the area to be software-protected against write instructions. These bits are written with the write status register (WRSR) instruction. When one or both of the block protect (BP1, BP0) bits is set to 1, the relevant memory area (as defined in Table 2) becomes protected against write instructions as defined in Table 3. The block protect (BP1, BP0) bits can be written provided that the hardware protected mode has not been set.

**Figure 9. Read Status Register (RDSR) sequence**



## 6.4 Write status register (WRSR)

The write status register (WRSR) instruction is used to write new values to the status register. Before it can be accepted, a write enable (WREN) instruction must have been previously executed.

The write status register (WRSR) instruction is entered by driving chip select ($\overline{S}$) low, followed by the instruction code, the data byte on serial data input (D) and chip select ($\overline{S}$) driven high. Chip select ($\overline{S}$) must be driven high after the rising edge of serial clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of serial clock (C). Otherwise, the write status register (WRSR) instruction is not executed.

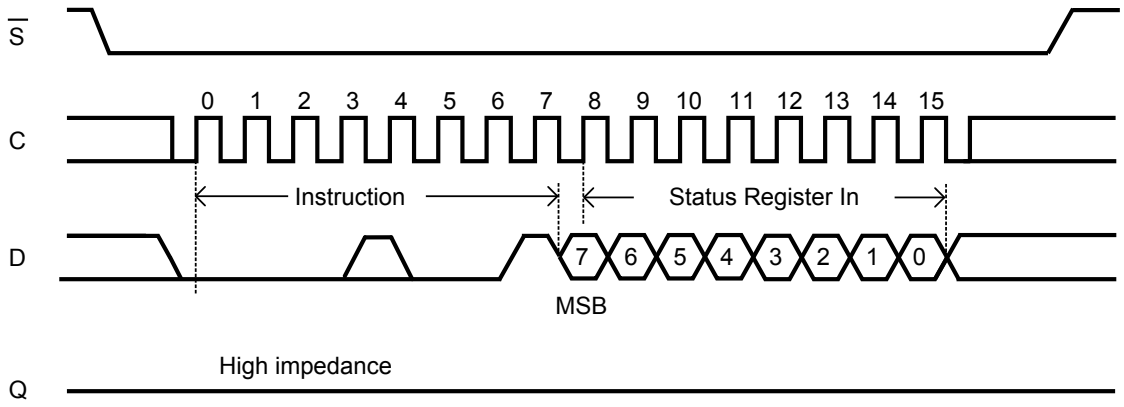
Driving the chip select ($\overline{S}$) signal high at a byte boundary of the input data triggers the self-timed write cycle that takes $t_W$ to complete (as specified in Table 17). The instruction sequence is shown in Figure 10.

While the write status register cycle is in progress, the status register may still be read to check the value of the write in progress (WIP) bit: the WIP bit is 1 during the self-timed write cycle $t_W$, and, 0 when the write cycle is complete. The WEL bit (write enable latch) is also reset at the end of the write cycle $t_W$.

The WRSR instruction allows the user to change the values of the BP1, BP0 bits, which define the size of the area that is to be treated as read only, as defined in Table 2. The contents of the BP1, BP0 bits are updated after the completion of the WRSR instruction, including the $t_W$ write cycle.

The WRSR instruction has no effect on the b7, b6, b5, b4, b1 and b0 bits in the status register. B7, b6, b5 and b4 are always read as 1.

**Figure 10. Write status register (WRSR) sequence**




The WRSR instruction is not accepted, and is not executed, under the following conditions:

- if the write enable latch (WEL) bit has not been set to 1 (by executing a write enable instruction just before)
- if a write cycle is already in progress
- if the device has not been deselected, by chip select ($\overline{S}$) being driven high, after the eighth bit, b0, of the data byte has been latched in
- if write protect ($\overline{W}$) is low during the WRSR command (instruction, address and data)

## 6.5 Read from memory array (READ)

As shown in Figure 11, to send this instruction to the device, chip select ($\overline{S}$) is first driven low. The bits of the instruction byte and address byte are then shifted in, on serial data input (D). For the M95040, the most significant address bit, A8, is incorporated as bit b3 of the instruction byte, as shown in Table 3. The address is loaded into an internal address register, and the byte of data at that address is shifted out, on serial data Output (Q).

If chip select ($\overline{S}$) continues to be driven low, an internal bit-pointer is automatically incremented at each clock cycle, and the corresponding data bit is shifted out.

When the highest address is reached, the address counter rolls over to zero, allowing the read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single read instruction.

The read cycle is terminated by driving chip select ($\overline{S}$) high. The rising edge of the chip select ($\overline{S}$) signal can occur at any time during the cycle.

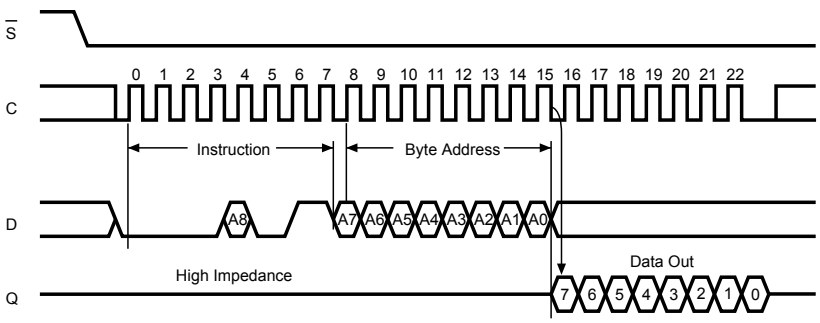
The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a write cycle is currently in progress.

**Table 6. Address range bits**

| Device | M95040 | M95020 | M95010 |
|---|---|---|---|
| Address bits | A8-A0 | A7-A0 | A6-A0 |

**Figure 11. Read from memory array (READ) sequence**




1. Depending on the memory size, as shown in Table 6, the most significant address bits are "Don't care".

## 6.6 Write to Memory array (WRITE)

As shown in Figure 12, to send this instruction to the device, chip select ($\overline{S}$) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on serial data input (D).

The instruction is terminated by driving chip select ($\overline{S}$) high at a byte boundary of the input data. The self-timed write cycle, triggered by the chip select ($\overline{S}$) rising edge, continues for a period $t_W$ (as specified in Table 17), at the end of which the write in progress (WIP) bit is reset to 0.

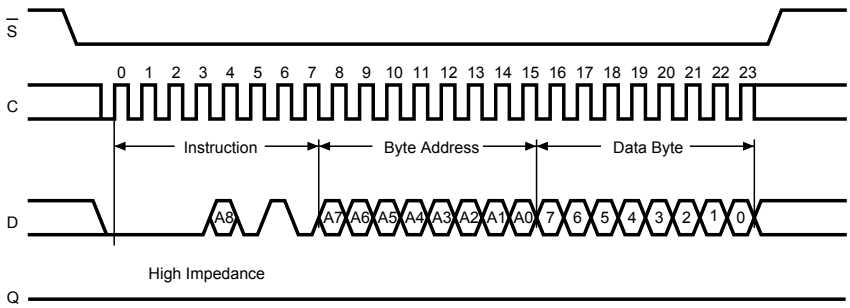
In the case of Figure 12, chip select ($\overline{S}$) is driven high after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. However, if chip select ($\overline{S}$) continues to be driven low (as shown in Figure 13), the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal write cycle. If chip select ($\overline{S}$) still continues to be driven low, the next byte of input data is shifted in, and used to overwrite the byte at the start of the current page.

The instruction is not accepted, and is not executed, under the following conditions:

- if the write enable latch (WEL) bit has not been set to 1 (by executing a write enable instruction just before)
- if a write cycle is already in progress
- if the device has not been deselected, by driving high chip select ($\overline{S}$), at a byte boundary (after the rising edge of Serial Clock (C) that latches the last data bit, and before the next rising edge of serial clock (C) occurs anywhere on the bus)
- if write protect ($\overline{W}$) is low or if the addressed page is in the area protected by the block brotect (BP1 and BP0) bits

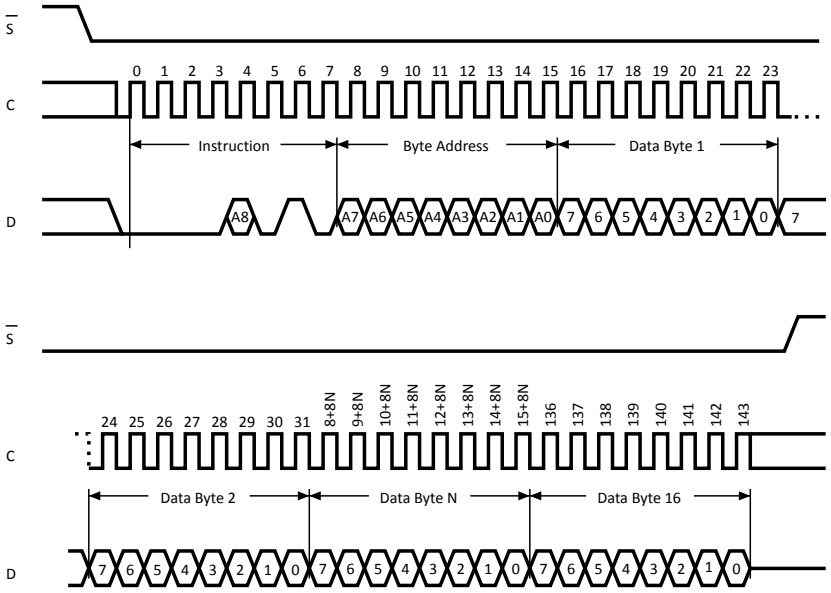
*Note: The self-timed write cycle $t_W$ is internally executed as a sequence of two consecutive events: [Erase addressed byte(s)], followed by [Program addressed byte(s)]. An erased bit is read as "0" and a programmed bit is read as "1".*

**Figure 12. Byte write (WRITE) sequence**




1. Depending on the memory size, as shown in Table 6, the most significant address bits are "Don't care".

**Figure 13. Page write (WRITE) sequence**




1. Depending on the memory size, as shown in Table 6, the most significant address bits are "Don't care".

## 6.7 Read identification page (available only in M95040-D device)

The read identification page (RDID) instruction is used to read the identification page (additional page of 16 bytes, which can be written and later permanently locked in read-only mode).

The chip select ($\overline{S}$) signal is first driven low, the bits of the instruction byte and address bytes are then shifted in (MSB first) on serial data input (D). Address bit A7 must be 0 and the other address bits are Don't Care except the lower address bits [A3:A0] (it might be easier to define these bits as 0, as shown in Table 3). Data is then shifted/clocked out (MSB first) on serial data output (Q).

The first byte addressed can be any byte within the identification page.

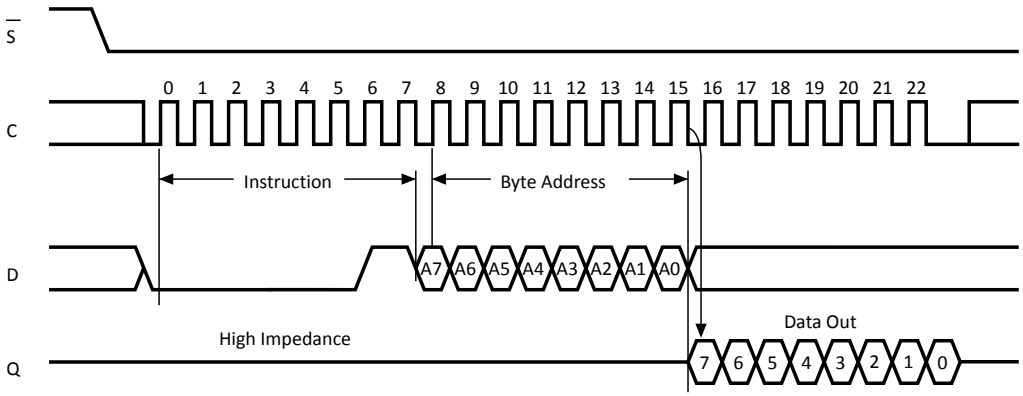
If chip select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented and the byte of data at the new address is shifted out.

Note that there is no roll over feature in the identification page. The address of bytes to read must not exceed the page boundary.

The read cycle is terminated by driving chip select ($\overline{S}$) high. The rising edge of the chip select ($\overline{S}$) signal can occur at any time during when the data bits are shifted out.

The instruction is not accepted, and is not executed, if a write cycle is currently in progress.

**Figure 14. Read identification page sequence**



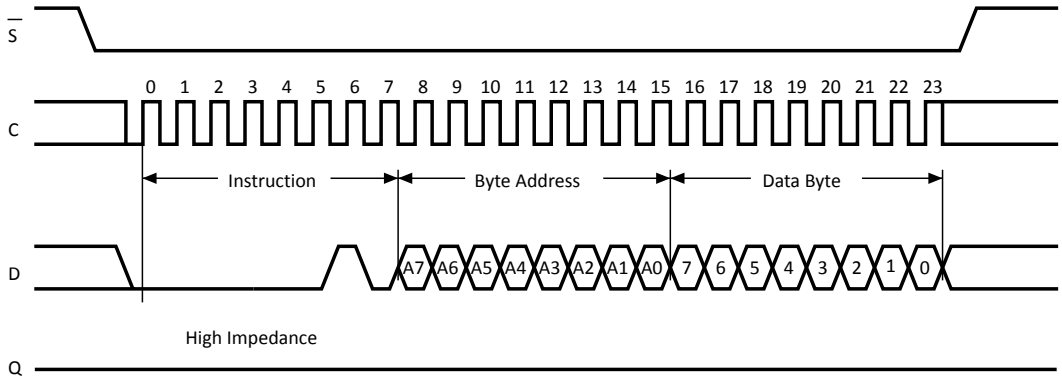
## 6.8 Write identification page (available only in M95040-D device)

The write identification page (WRID) instruction is used to write the identification page (additional page of 16 bytes which can also be permanently locked in read-only mode).

The chip select signal ($\overline{S}$) is first driven low, and then the bits of the instruction byte, address bytes, and at least one data byte are shifted in (MSB first) on serial data input (D). Address bit A7 must be 0 and the other address bits are Don't Care except the lower address bits [A3:A0] (it might be easier to define these bits as 0, as shown in Table 3).

The self-timed write cycle starts from the rising edge of chip select ($\overline{S}$), and continues for a period $t_W$ (as specified in Section 9 DC and AC parameters).

**Figure 15. Write identification page sequence**




The instruction is discarded, and is not executed if the block protect bits (BP1,BP0) = (1,1) or one of the conditions defined in Section 5.4 Data protection and protocol control is not satisfied.

## 6.9 Read lock status (available only in M95040-D device)

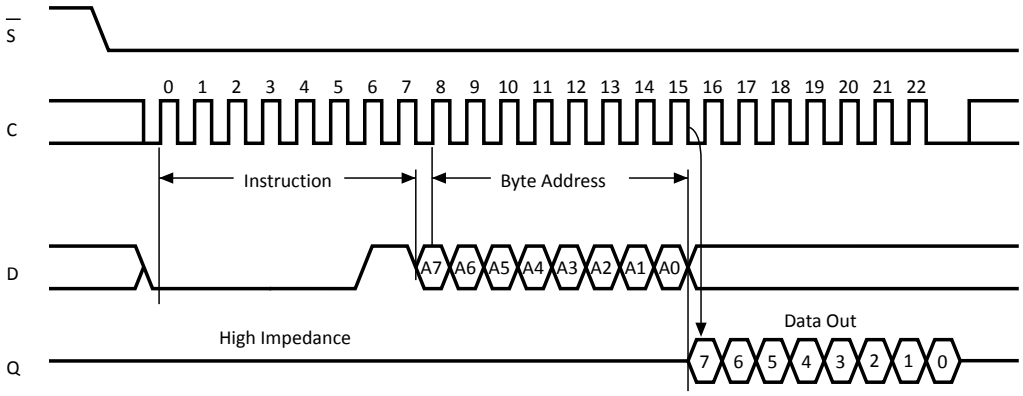
The read lock status (RDLS) instruction is used to read the lock status.

To send this instruction to the device, chip select ($\overline{S}$) first has to be driven low. The bits of the instruction byte and address bytes are then shifted (MSB first) in on serial data input (D). Address bit A7 must be 1, all other address bits are Don't Care (it might be easier to define these bits as 0, as shown in Table 3). The lock bit is the LSB (least significant bit) of the byte read on serial data output (Q). It is at “1” when the lock is active and at “0” when the lock is not active. If chip select ($\overline{S}$) continues to be driven low, the same data byte is shifted out.

The read cycle is terminated by driving chip select ($\overline{S}$) high. The instruction sequence is shown in Figure 16.

The read lock status instruction is not accepted and not executed if a write cycle is currently in progress.

**Figure 16. Read lock status sequence**

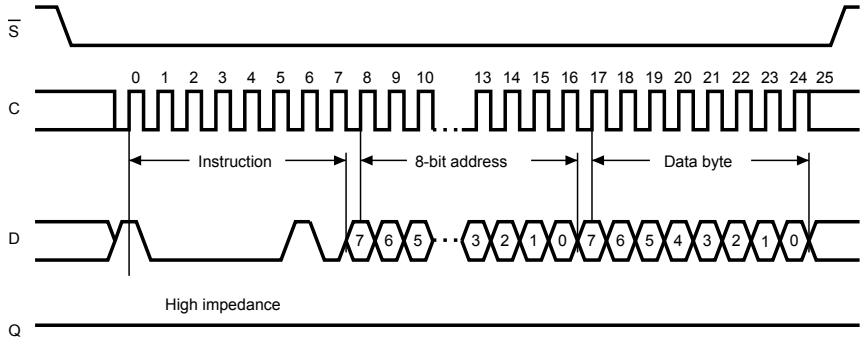


## 6.10 Lock identification page (available only in M95040-D device)

The lock identification page (LID) instruction permanently locks the identification page in read-only mode.

The LID instruction is issued by driving chip select ($\overline{S}$) low, sending (MSB first) the instruction code, the address and a data byte on serial data input (D), and driving chip select ($\overline{S}$) high. In the address sent, A7 must be equal to 1, all other address bits are Don't Care (it might be easier to define these bits as 0, as shown in Table 3). The data byte sent must be equal to the binary value xxxx xx1x, where x = Don't Care. The LID instruction is terminated by driving Chip Select (S) high at a data byte boundary, otherwise, the instruction is not executed.

**Figure 17. Lock ID sequence**




Driving chip select ($\overline{S}$) high at a byte boundary of the input data triggers the self-timed write cycle whose duration is $t_W$ (as specified in AC characteristics in Section 9 DC and AC parameters). The instruction sequence is shown in Figure 17.

The instruction is discarded, and is not executed if the block protect bits (BP1,BP0) = (1,1) or one of the conditions defined in Section 5.4 Data protection and protocol control is not satisfied.

# 7 Power-up and delivery state

## 7.1 Power-up state

After power-up, the device is in the following state:

- Standby power mode
- Deselected (after power-up, a falling edge is required on chip select ($\overline{S}$) before any instructions can be started)
- Not in the hold condition
- The write enable latch (WEL) is reset to 0
- Write in progress (WIP) is reset to 0

The BP1 and BP0 bits of the status register are unchanged from the previous power-down (they are non-volatile bits).

## 7.2 Initial delivery state

The device is delivered with:

- The memory array set to all 1s (each byte = FFh)
- The block protect (BP1 and BP0) bits are initialized to 0
- The identification page bits, for M95040-D only, set to all 1s (each byte = FFh)

# 8 Maximum ratings

Stressing the device outside the ratings listed in Table 7 may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 7. Absolute maximum ratings**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_{AMB}$ | Ambient operating temperature | –40 | 130 | °C |
| $T_{STG}$ | Storage temperature | –65 | 150 | |
| $T_{LEAD}$ | Lead temperature during soldering | See note (1) | | |
| $V_O$ | Output voltage | –0.50 | $V_{CC}$ + 0.6 | V |
| $V_I$ | Input voltage | –0.50 | $V_{CC}$ + 1.0 | |
| $I_{OL}$ | DC output current (Q = 0) | - | 5 | mA |
| $I_{IH}$ | DC output current (Q = 1) | - | 5 | |
| $V_{CC}$ | Supply voltage | -0.50 | 6.5 | V |
| $V_{ESD}$ | Electrostatic discharge voltage (human body model) (2) | - | 4000 | V |

1. *Compliant with JEDEC standard J-STD-020 (for small-body, Sn-Pb or Pb free assembly), the ST ECOPACK 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS directive 2011/65/EU of July 2011).*
2. *Positive and negative pulses applied on different combinations of pin connections, according to AEC-Q100-002 (compliant with ANSI/ESDA/JEDEC JS-001, C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω).*

# 9 DC and AC parameters

This section summarizes the operating and measurement conditions and the DC/AC characteristics of the device.

**Table 8. Operating conditions (M950x0-W)**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 2.5 | 5.5 | V |
| $T_A$ | Ambient operating temperature | –40 | 85 | °C |

**Table 9. Operating conditions (M950x0-R)**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 1.8 | 5.5 | V |
| $T_A$ | Ambient operating temperature | -40 | 85 | °C |

**Table 10. Operating conditions (M95040-DF)**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 1.7 | 5.5 | V |
| $T_A$ | Ambient operating temperature | –40 | 85 | °C |

**Table 11. AC measurement conditions**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_L$ | Load capacitance | - | 30 | pF |
| - | Input rise and fall times | - | 50 | ns |
| - | Input levels | 0.2 $V_{CC}$ to 0.8 $V_{CC}$ | | V |
| - | Input and output timing references voltages | 0.3 $V_{CC}$ to 0.7 $V_{CC}$ | | V |

**Figure 18. AC measurement I/O waveform**

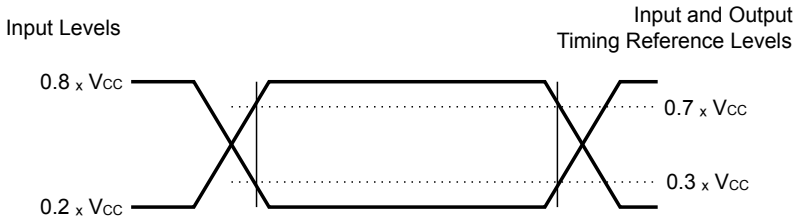


**Table 12. Cycling performance**

| Symbol | Parameter | Test condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $N_{cycle}$ | Write cycle endurance | $T_A \leq 25$ °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$ | - | 4,000,000 | Write cycle(1) |
| | | $T_A = 85$ °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$ | - | 1,200,000 | |

1. *A Write cycle is executed when either a page write, a byte write, a WRSR, a WRID or an LID instruction is decoded. When using the byte write, the page write or the WRID instruction, refer also to Section 5.5 Error correction code (ECC x 1) .*

**Table 13. Memory cell data retention**

| Parameter | Test condition | Min. | Max. | Unit |
|---|---|---|---|---|
| Data retention(1) | $T_A = 55$ °C | - | 200 | Year |

1. *The data retention behavior is checked in production, while the 200-year limit is defined from characterization and qualification results.*

**Table 14. Capacitance**

| Symbol(1) | Parameter | Test condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{OUT}$ | Output capacitance (Q) | $V_{OUT} = 0$ V | - | 8 | pF |
| $C_{IN}$ | Input capacitance (D) | $V_{IN} = 0$ V | - | 8 | pF |
| | Input capacitance (other pins) | $V_{IN} = 0$ V | - | 6 | pF |

1. *Sampled only, not 100% tested, at TA=25 °C and a frequency of 5 MHz*

**Table 15. DC characteristics (M950x0-W)**

| Symbol | Parameter | Test conditions in addition to those defined in Table 8 and Table 11 | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input leakage current | $V_{IN} = V_{SS}$ or $V_{CC}$ | - | ± 2 | µA |
| $I_{LO}$ | Output leakage current | $\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or $V_{CC}$ | - | ± 2 | µA |
| $I_{CC}$ | Supply current (Read) | $V_{CC}$= 2.5 V, C= 0.1 $V_{CC}$ / 0.9 $V_{CC}$ at $f_C$ = 5 MHz, Q = open | - | 2 | mA |
| | | $V_{CC}$= 2.5 V, C = 0.1 $V_{CC}$ / 0.9 $V_{CC}$ at $f_C$ = 10 MHz, Q = open | - | 2 | |
| | | $V_{CC}$= 5.5 V, C = 0.1 $V_{CC}$ / 0.9 $V_{CC}$ at $f_C$ = 20 MHz, Q = open | - | 5 | |
| $I_{CC0}$ (1) | Supply current (Write) | During $t_W$, $\overline{S} = V_{CC}$, 2.5 V ≤ $V_{CC}$ < 5.5 V | - | 5 | mA |
| $I_{CC1}$ | Supply current (Standby Power mode) | $\overline{S} = V_{CC}$, $V_{CC}$= 5.5 V, $V_{IN} = V_{SS}$ or $V_{CC}$ | - | 3 | µA |
| | | $\overline{S} = V_{CC}$, $V_{CC}$= 2.5 V, $V_{IN} = V_{SS}$ or $V_{CC}$ | - | 2 | |
| $V_{IL}$ | Input low voltage | - | –0.45 | 0.3 $V_{CC}$ | V |
| $V_{IH}$ | Input high voltage | - | 0.7 $V_{CC}$ | $V_{CC}$+1 | V |
| $V_{OL}$ | Output low voltage | $V_{CC}$ = 2.5 V and $I_{OL}$ = 1.5 mA | - | 0.4 | V |
| $V_{OH}$ | Output high voltage | $V_{CC}$ = 2.5 V and $I_{OH}$ = 0.4 mA or $V_{CC}$ = 5 V and $I_{OH}$ = 2 mA | 0.8 $V_{CC}$ | - | V |
| $V_{RES}$(1) | Internal reset threshold voltage | - | 0.5 | 1.5 | V |

1. *Evaluated by characterization - not tested in production.*

**Table 16. DC characteristics (M950x0-R or M950x0-DF)**

| Symbol | Parameter | Test conditions in addition to those defined in Table 9, Table 10 and Table 11 | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input leakage current | $V_{IN} = V_{SS}$ or $V_{CC}$ | - | ± 2 | µA |
| $I_{LO}$ | Output leakage current | $\overline{S} = V_{CC}$, voltage applied on Q = $V_{SS}$ or $V_{CC}$ | - | ± 2 | µA |
| $I_{CC}$ | Supply current (Read) | $V_{CC}$= 1.8 V or 1.7 V, C = 0.1 $V_{CC}$ or 0.9 $V_{CC}$<br>at $f_C$ = 5 MHz , Q = open | - | 2 | mA |
| $I_{CC0}$ (2) | Supply current (Write) | $V_{CC}$ = 1.8 V or 1.7 V, during $t_W$, $\overline{S} = V_{CC}$ | - | 5 | mA |
| $I_{CC1}$ | Supply current (Standby Power mode) | $V_{CC}$ = 1.8 V or 1.7 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or $V_{CC}$ | - | 1 | µA |
| $V_{IL}$ | Input low voltage | $V_{CC}$ < 2.5 V | –0.45 | 0.25 $V_{CC}$ | V |
| $V_{IH}$ | Input high voltage | $V_{CC}$ < 2.5 V | 0.75 $V_{CC}$ | $V_{CC}$+1 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 0.15 mA, $V_{CC}$ = 1.8 V or 1.7 V | - | 0.3 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = –0.1 mA, $V_{CC}$ = 1.8 V or 1.7 V | 0.8 $V_{CC}$ | - | V |
| $V_{RES}$ (2) | Internal reset threshold voltage | - | 0.5 | 1.5 | V |

1. *If the application uses the M950x0-R or M95040-DF devices with 2.5 V ≤ $V_{CC}$ ≤ 5.5 V and -40 °C ≤ TA ≤ +85 °C, refer to Table 15.*
2. *Evaluated by characterization - not tested in production.*

**Table 17. AC characteristics**

| Test conditions specified in Table 8, Table 9, Table 10 and Table 11 | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Symbol | Alt. | Parameter | $V_{CC}$ ≥ 1.7 V or 1.8 V | | $V_{CC}$ ≥ 2.5$V_{CC}$ | | $V_{CC}$ ≥ 4.5V | | Unit |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $f_C$ | $f_{SCK}$ | Clock frequency | D.C. | 5 | D.C. | 10 | D.C. | 20 | MHz |
| $t_{SLCH}$ | $t_{CSS1}$ | $\overline{S}$ active setup time | 60 | - | 30 | - | 15 | - | ns |
| $t_{SHCH}$ | $t_{CSS2}$ | $\overline{S}$ not active setup time | 60 | - | 30 | - | 15 | - | ns |
| $t_{SHSL}$ | $t_{CS}$ | $\overline{S}$ deselect time | 90 | - | 40 | - | 20 | - | ns |
| $t_{CHSH}$ | $t_{CSH}$ | $\overline{S}$ active hold time | 60 | - | 30 | - | 15 | - | ns |
| $t_{CHSL}$ | - | $\overline{S}$ not active hold time | 60 | - | 30 | - | 15 | - | ns |
| $t_{CH}$ (1) | $t_{CLH}$ | Clock high time | 80 | - | 40 | - | 20 | - | ns |
| $t_{CL}$ (1) | $t_{CLL}$ | Clock low time | 80 | - | 40 | - | 20 | - | ns |
| $t_{CLCH}$ (2) | $t_{RC}$ | Clock rise time | - | 2 | - | 2 | - | 2 | µs |
| $t_{CHCL}$ (2) | $t_{FC}$ | Clock fall time | - | 2 | - | 2 | - | 2 | µs |
| $t_{DVCH}$ | $t_{DSU}$ | Data in setup time | 20 | - | 10 | - | 5 | - | ns |
| $t_{CHDX}$ | $t_{DH}$ | Data in hold time | 20 | - | 10 | - | 10 | - | ns |
| $t_{HHCH}$ | - | Clock low hold time after $\overline{HOLD}$ not active | 60 | - | 30 | - | 15 | - | ns |
| $t_{HLCH}$ | - | Clock low hold time after $\overline{HOLD}$ active | 60 | - | 30 | - | 15 | - | ns |
| $t_{CLHL}$ | - | Clock low setup time before $\overline{HOLD}$ active | 0 | - | 0 | - | 0 | - | ns |
| $t_{CLHH}$ | - | Clock low setup time before $\overline{HOLD}$ not active | 0 | - | 0 | - | 0 | - | ns |
| $t_{SHQZ}$ (2) | $t_{DIS}$ | Output disable time | - | 80 | - | 40 | - | 20 | ns |
| $t_{CLQV}$ (3) | $t_V$ | Clock low to output valid | - | 80 | - | 40 | - | 20 | ns |
| $t_{CLQX}$ | $t_{HO}$ | Output hold time | 0 | - | 0 | - | 0 | - | ns |
| $t_{QLQH}$ (2) | $t_{RO}$ | Output rise time | - | 80 | - | 40 | - | 20 | ns |
| $t_{QHQL}$ (2) | $t_{FO}$ | Output fall time | - | 80 | - | 40 | - | 20 | ns |
| $t_{HHQV}$ | $t_{LZ}$ | $\overline{HOLD}$ high to output valid | - | 80 | - | 40 | - | 20 | ns |
| $t_{HLQZ}$ (2) | $t_{HZ}$ | $\overline{HOLD}$ low to output High-Z | - | 80 | - | 40 | - | 20 | ns |
| $t_W$ | $t_{WC}$ | Write time | - | 5 | - | 5 | - | 5 | ms |

1. *$t_{CH}$ + $t_{CL}$ must never be less than the shortest possible clock period, 1 / $f_C$(max).*
2. *Evaluated by characterization - not tested in production.*
3. *$t_{CLQV}$ must be compatible with $t_{CL}$ (clock low time): if the SPI bus master offers a read setup time $t_{SU}$ = 0 ns, $t_{CL}$ can be equal to (or greater than) $t_{CLQV}$; in all other cases, $t_{CL}$ must be equal to (or greater than) $t_{CLQV}$+$t_{SU}$.*

Figure 19. **Serial input timing**

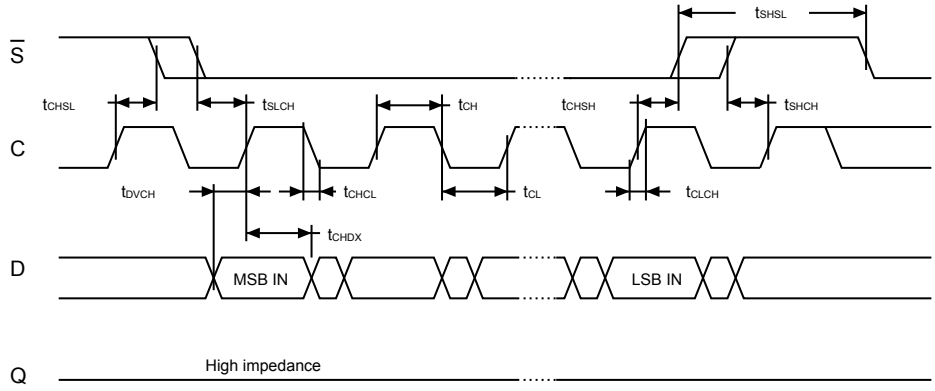



Figure 20. **Hold timing**

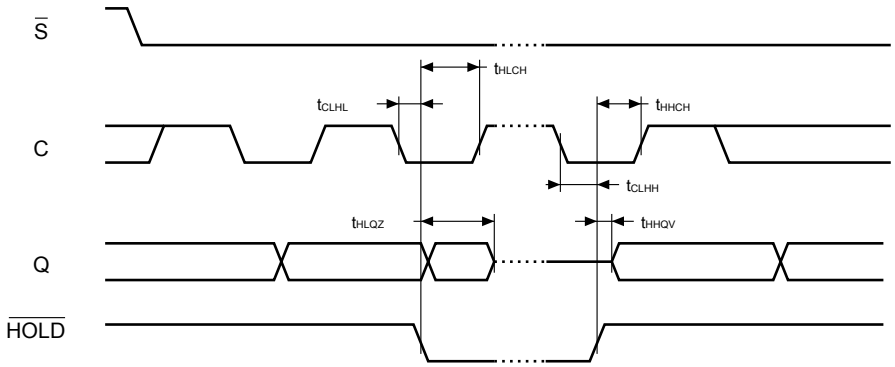
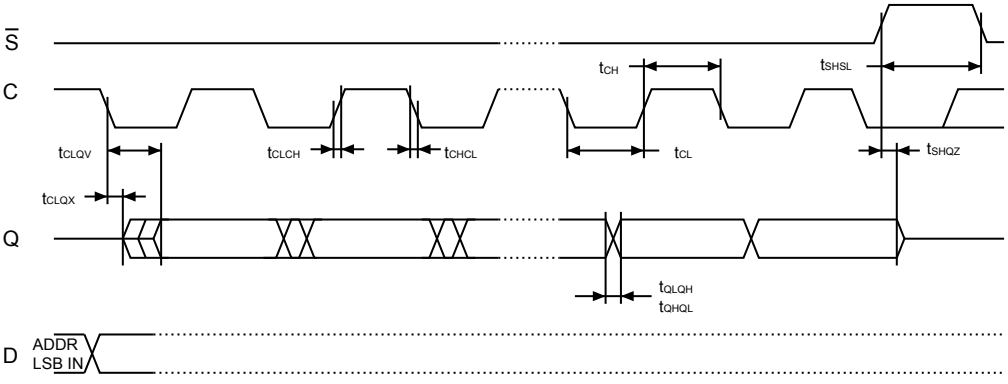



Figure 21. **Serial output timing**



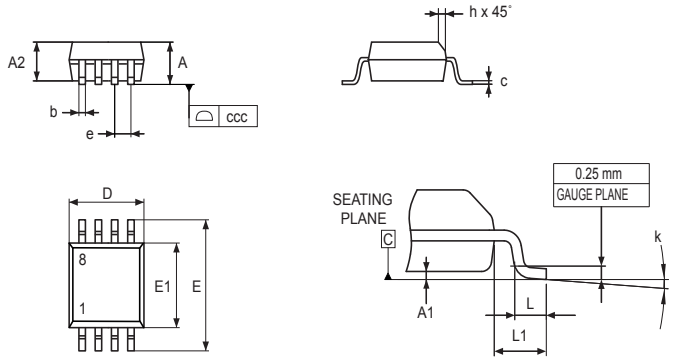
# 10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 10.1 SO8N package information

This SO8N is an 8-lead, 4.9 x 6 mm, plastic small outline, 150 mils body width, package.

**Figure 22. SO8N – Outline**



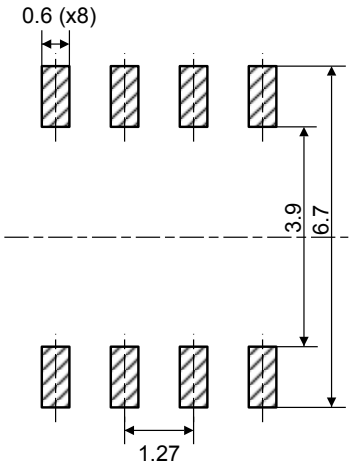

1. Drawing is not to scale.

**Table 18. SO8N – Mechanical data**

| Symbol | millimeters | | | inches (1) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | - | - | 1.750 | - | - | 0.0689 |
| A1 | 0.100 | - | 0.250 | 0.0039 | - | 0.0098 |
| A2 | 1.250 | - | - | 0.0492 | - | - |
| b | 0.280 | - | 0.480 | 0.0110 | - | 0.0189 |
| c | 0.100 | - | 0.230 | 0.0030 | - | 0.0091 |
| D(2) | 4.800 | 4.900 | 5.000 | 0.1890 | 0.1929 | 0.1969 |
| E | 5.800 | 6.000 | 6.200 | 0.2283 | 0.2362 | 0.2441 |
| E1(3) | 3.800 | 3.900 | 4.000 | 0.1496 | 0.1535 | 0.1575 |
| e | - | 1.270 | - | - | 0.0500 | - |
| h | 0.250 | - | 0.500 | 0.0098 | - | 0.0197 |
| k | 0° | - | 8° | 0° | - | 8° |
| L | 0.400 | - | 1.270 | 0.0157 | - | 0.0500 |
| L1 | - | 1.040 | - | - | 0.0409 | - |
| ccc | - | - | 0.100 | - | - | 0.0039 |

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side*
3. *Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.*

Figure 23. **SO8N - Recommended footprint**

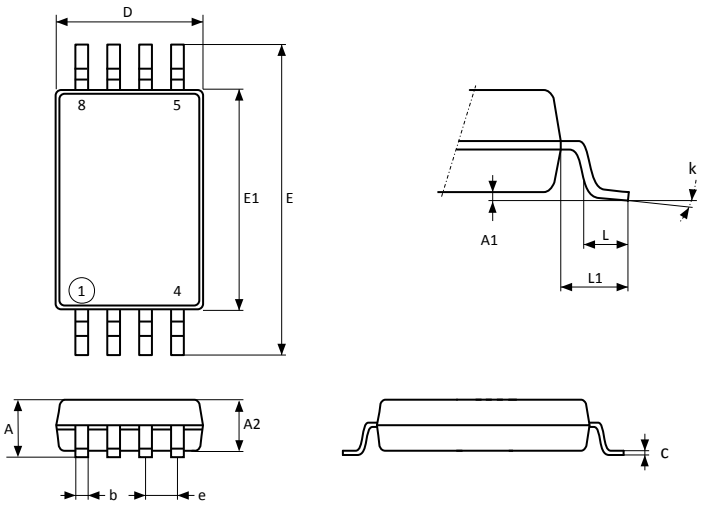



1. Dimensions are expressed in millimeters.

## 10.2 TSSOP8 package information

This TSSOP is an 8-lead, 3 x 6.4 mm, 0.65 mm pitch, thin shrink small outline package.

**Figure 24. TSSOP8 – Outline**



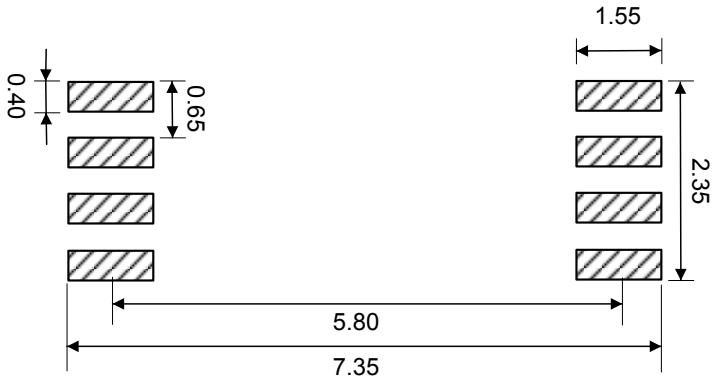

1. Drawing is not to scale.

**Table 19. TSSOP8 – Mechanical data**

| Symbol | millimeters | | | inches [1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | - | - | 1.200 | - | - | 0.0472 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 0.800 | 1.000 | 1.050 | 0.0315 | 0.0394 | 0.0413 |
| b | 0.190 | - | 0.300 | 0.0075 | - | 0.0118 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D[2] | 2.900 | 3.000 | 3.100 | 0.1142 | 0.1181 | 0.1220 |
| e | - | 0.650 | - | - | 0.0256 | - |
| E | 6.200 | 6.400 | 6.600 | 0.2441 | 0.2520 | 0.2598 |
| E1[3] | 4.300 | 4.400 | 4.500 | 0.1693 | 0.1732 | 0.1772 |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | - | 8° | 0° | - | 8° |
| aaa | - | - | 0.100 | - | - | 0.0039 |

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side*
3. *Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.*

Figure 25. **TSSOP8 – Recommended footprint**

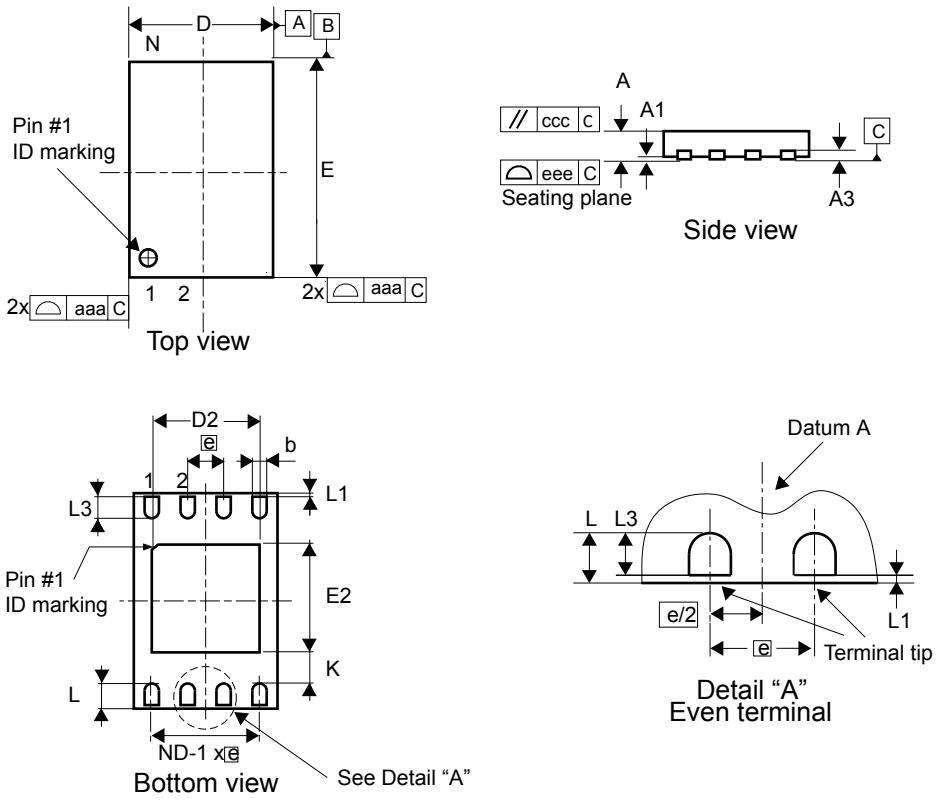



1. Dimensions are expressed in millimeters.

## 10.3 UFDFPN8 (DFN8) package information

This UFDFPN is a 8-lead, 2 x 3 mm, 0.5 mm pitch ultra thin profile fine pitch dual flat package.

**Figure 26. UFDFPN8 - Outline**



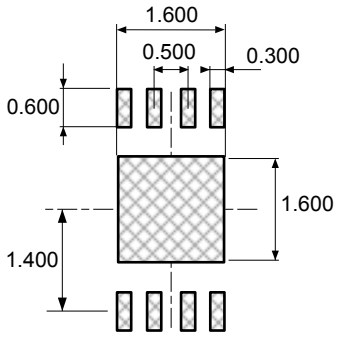

1. Maximum package warpage is 0.05 mm.
2. Exposed copper is not systematic and can appear partially or totally according to the cross section.
3. Drawing is not to scale.
4. The central pad (the area E2 by D2 in the above illustration) must be either connected to $V_{SS}$ or left floating (not connected) in the end application.

**Table 20. UFDFPN8 - Mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.450 | 0.550 | 0.600 | 0.0177 | 0.0217 | 0.0236 |
| A1 | 0.000 | 0.020 | 0.050 | 0.0000 | 0.0008 | 0.0020 |
| b[2] | 0.200 | 0.250 | 0.300 | 0.0079 | 0.0098 | 0.0118 |
| D | 1.900 | 2.000 | 2.100 | 0.0748 | 0.0787 | 0.0827 |
| D2 | 1.200 | - | 1.600 | 0.0472 | - | 0.0630 |
| E | 2.900 | 3.000 | 3.100 | 0.1142 | 0.1181 | 0.1220 |
| E2 | 1.200 | - | 1.600 | 0.0472 | - | 0.0630 |
| e | - | 0.500 | - | - | 0.0197 | - |
| K | 0.300 | - | - | 0.0118 | - | - |
| L | 0.300 | - | 0.500 | 0.0118 | - | 0.0197 |
| L1 | - | - | 0.150 | - | - | 0.0059 |
| L3 | 0.300 | - | - | 0.0118 | - | - |
| aaa | - | - | 0.150 | - | - | 0.0059 |
| bbb | - | - | 0.100 | - | - | 0.0039 |
| ccc | - | - | 0.100 | - | - | 0.0039 |
| ddd | - | - | 0.050 | - | - | 0.0020 |
| eee[3] | - | - | 0.080 | - | - | 0.0031 |

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension b applies to plated terminal and is measured between 0.15 and 0.30 mm from the terminal tip.*
3. *Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.*

**Figure 27. UFDFPN8 - Recommended footprint**




1. Dimensions are expressed in millimeters.

# 11 Ordering information

**Table 21. Ordering information scheme**

Example: M95 040-D W MN 6 T P

**Device type**

M95 = SPI serial access EEPROM

**Device function**

040 = 4 Kbit (512 x 8)

040-D = 4 Kbit (512 x 8) plus identification page

020 = 2 Kbit (256 x 8)

010 = 1 Kbit (128 x 8)

**Operating voltage**

W = $V_{CC}$ = 2.5 to 5.5 V

R = $V_{CC}$ = 1.8 to 5.5 V

F = $V_{CC}$ = 1.7 to 5.5 V

**Package**(1)

MN = SO8 (150 mil width)

DW = TSSOP8 (169 mil width)

MC = UFDFPN8 (DFN8)

**Device grade**

6 = Industrial temperature range, –40 to 85 °C

Device tested with standard test flow

**Option**

blank = tube packing

T = Tape and reel packing

**Plating technology**

G or P = RoHS compliant and halogen-free (ECOPACK2)

1. *All packages are ECOPACK2 (RoHS-compliant and free of brominated, chlorinated and antimony-oxide flame retardants).*

*Note: For a list of available options (memory, package, and so on) or for further information on any aspect of this device, contact your nearest ST sales office.*

*Note: Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.*

## Revision history

Table 22. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 02-Feb-2012 | 10 | Document renamed from “M95040 M95020 M95010” to “M950x0 M950x0-W M950x0-R”<br>Silhouette of UDFPN8 (MB or MC) on the cover page updated.<br>*Section6.3: Read Status Register (RDSR)*updated. Text modified in *Section6.3.1: WIPbit*.<br>*Table8:Absolutemaximum ratings* updated.<br>*Figure24:UFDFPN8(MLP8) 8-leadultrathin finepitchdualflatpackagenolead 2 × 3mm, outline* modified.<br>*Table24: UFDFPN8 (MLP8)8-leadultra thinfine pitch dual flat package no lead 2 × 3mm, data* updated.<br>Removed tables of available products from *Section 11: Part numbering*. |
| 24-May-2013 | 11 | Document renamed from “M95040 M95020 M95010” to “M950x0-W M950x0-R”.<br>Silhouette of UDFPN8 (MB or MC) on the cover page updated.<br>*Section6.3: Read Status Register (RDSR)*updated. Text modified in *Section6.3.1: WIPbit*.<br>*Table8*and *Table24* updated.<br>Tables 8, 13, 15, 17, 19 removed.<br>*Figure24*modified.<br>Removed tables of available products from *Section 11: Part numbering*. |
| 17-Oct-2013 | 12 | Added “M95040-DF” part number. Updated:<br>Updated:<br>• Features: Single supply voltage, high-speed clock frequency, memory array, write cycles and data retention<br>• Section 1: Description<br>• Figure 6: Block diagram<br>• Section 6: Instructions: updated introduction and added Section 6.7 to Section 6.10<br>• Section 7.2: Initial delivery state<br>• Note (1) under Table 8: Absolute maximum ratings.<br>• Table 16: DC characteristics (M950x0-W, device grade 6), Table 18: AC characteristics (M950x0-W, device grade 6) and Table 25: Ordering information scheme<br>Added Table 13: Cycling performance, Table 14: Memory cell data retention, Table 17: DC characteristics (M950x0-R or M95040-DF, device grade 6) and Table 19: AC characteristics (M950x0-R or M95040-DF, device grade 6).<br>Renamed Table 20 and Table 21. |
| 28-Aug-2014 | 13 | Updated footnotes:<br>• 1 in Table 13: Cycling performance;<br>• 1 in Table 14: Memory cell data retention;<br>• 2 in Table 19: AC characteristics (M950x0-R or M95040-DF, device grade 6);<br>• 2 in Table 21: AC characteristics (M950x0-R, device grade 6).<br>Updated Table 20 with new title AC characteristics (M950x0-W, device grade 6) and addition of footnote 1.<br>Updated Table 21 with new title AC characteristics (M950x0-R, device grade 6) and addition of footnote 1.<br>Updated Table 25: Ordering information scheme. |

| Date | Version | Changes |
|---|---|---|
| 05-Apr-2022 | 14 | Updated:<br>• Section Features, Section 2 Block diagram, Section 3.8 VSS ground, Section 4 Connecting to the SPI bus, Section 5.1 Supply voltage (VCC) and its subsection, Section 7.1 Power-up state, Section 7.2 Initial delivery state, Section 10.1 SO8N package information, Section 10.2 TSSOP8 package information<br>• Notes 1 and 2 of Table 7. Absolute maximum ratings, note of Table 12. Cycling performance, note of Table 13. Memory cell data retention,<br>• Table 11. AC measurement conditions, Table 15. DC characteristics (M950x0-W), Table 16. DC characteristics (M950x0-R or M950x0-DF), Table 17. AC characteristics, Table 21. Ordering information scheme<br>Added:<br>• Section 3.7 VCC supply voltage, Section 5.5 Error correction code (ECC x 1)<br>Removed: Table 19. AC characteristics (M950x0-R or M95040-DF, device grade 6), Table 20. AC characteristics (M950x0-W, device grade 6), Table 21. AC characteristics (M950x0-R, device grade 6) |

# Contents

1 **Description** . . . . 2
2 **Block diagram** . . . . 4
3 **Signal description** . . . . 5
3.1 Serial data output (Q) . . . . 5
3.2 Serial data input (D) . . . . 5
3.3 Serial clock (C) . . . . 5
3.4 Chip select ($\overline{S}$) . . . . 5
3.5 Hold ($\overline{HOLD}$) . . . . 5
3.6 Write protect ($\overline{W}$) . . . . 5
3.7 $V_{CC}$ supply voltage . . . . 5
3.8 $V_{SS}$ ground . . . . 5
4 **Connecting to the SPI bus** . . . . 6
4.1 SPI modes . . . . 7
5 **Operating features** . . . . 8
5.1 Supply voltage ($V_{CC}$) . . . . 8
5.1.1 Operating supply voltage ($V_{CC}$) . . . . 8
5.1.2 Device reset . . . . 8
5.1.3 Power-up conditions . . . . 8
5.1.4 Power-down . . . . 8
5.1.5 Active power and Standby power modes . . . . 8
5.2 Hold condition . . . . 9
5.3 Status register . . . . 9
5.4 Data protection and protocol control . . . . 10
5.5 Error correction code (ECC x 1) . . . . 11
6 **Instructions** . . . . 12
6.1 Write enable (WREN) . . . . 13
6.2 Write disable (WRDI) . . . . 14
6.3 Read Status register (RDSR) . . . . 15
6.3.1 WIP bit . . . . 15
6.3.2 WEL bit . . . . 15
6.3.3 BP1, BP0 bits . . . . 16
6.4 Write status register (WRSR) . . . . 17
6.5 Read from memory array (READ) . . . . 18
6.6 Write to Memory array (WRITE) . . . . 19

6.7 Read identification page (available only in M95040-D device) . . . . . 21
6.8 Write identification page (available only in M95040-D device) . . . . . 22
6.9 Read lock status (available only in M95040-D device) . . . . . 23
6.10 Lock identification page (available only in M95040-D device) . . . . . 24
**7 Power-up and delivery state . . . . . 25**
7.1 Power-up state . . . . . 25
7.2 Initial delivery state . . . . . 25
**8 Maximum ratings . . . . . 26**
**9 DC and AC parameters . . . . . 27**
**10 Package information . . . . . 33**
10.1 SO8N package information . . . . . 33
10.2 TSSOP8 package information . . . . . 35
10.3 UFDFPN8 (DFN8) package information . . . . . 37
**11 Ordering information . . . . . 39**
**Revision history . . . . . 40**

# List of tables

Table 1. Signal names . . . 2
Table 2. Write-protected block size . . . 10
Table 3. Instruction set . . . 12
Table 4. Significant bits within the address bytes . . . 12
Table 5. Status register format . . . 15
Table 6. Address range bits . . . 18
Table 7. Absolute maximum ratings . . . 26
Table 8. Operating conditions (M950x0-W) . . . 27
Table 9. Operating conditions (M950x0-R) . . . 27
Table 10. Operating conditions (M95040-DF) . . . 27
Table 11. AC measurement conditions . . . 27
Table 12. Cycling performance . . . 28
Table 13. Memory cell data retention . . . 28
Table 14. Capacitance . . . 28
Table 15. DC characteristics (M950x0-W) . . . 29
Table 16. DC characteristics (M950x0-R or M950x0-DF) . . . 30
Table 17. AC characteristics . . . 31
Table 18. SO8N – Mechanical data . . . 33
Table 19. TSSOP8 – Mechanical data . . . 35
Table 20. UFDFPN8 - Mechanical data . . . 38
Table 21. Ordering information scheme . . . 39
Table 22. Document revision history . . . 40

# List of figures

Figure 1. Logic diagram. . . . 2
Figure 2. 8-pin package connections (top view) . . . 3
Figure 3. Block diagram . . . 4
Figure 4. Bus master and memory devices on the SPI bus. . . . 6
Figure 5. SPI modes supported . . . 7
Figure 6. Hold condition activation . . . 9
Figure 7. Write enable (WREN) sequence . . . 13
Figure 8. Write disable (WRDI) sequence . . . 14
Figure 9. Read Status Register (RDSR) sequence . . . 16
Figure 10. Write status register (WRSR) sequence . . . 17
Figure 11. Read from memory array (READ) sequence . . . 18
Figure 12. Byte write (WRITE) sequence . . . 19
Figure 13. Page write (WRITE) sequence . . . 20
Figure 14. Read identification page sequence . . . 21
Figure 15. Write identification page sequence . . . 22
Figure 16. Read lock status sequence . . . 23
Figure 17. Lock ID sequence . . . 24
Figure 18. AC measurement I/O waveform . . . 27
Figure 19. Serial input timing . . . 32
Figure 20. Hold timing. . . . 32
Figure 21. Serial output timing . . . 32
Figure 22. SO8N – Outline . . . 33
Figure 23. SO8N - Recommended footprint . . . 34
Figure 24. TSSOP8 – Outline . . . 35
Figure 25. TSSOP8 – Recommended footprint. . . . 36
Figure 26. UFDFPN8 - Outline . . . 37
Figure 27. UFDFPN8 - Recommended footprint . . . 38